SHRI RAMDEOBABA COLLEGE OF ENGINEERING AND MANAGEMENT, NAGPUR

An Autonomous College of Rashtrasant Tukadoji Maharaj
Nagpur University, Nagpur, Maharashtra, India

TEACHING SCHEME & SYLLABUS 2014-15

M TECH VLSI DESIGN

Published by
Dr. R.S. Pande
Principal
Shri Ramdeobaba College of Engineering & Management
Ramdeo Tekdi, Gittikhadan, Katol Road, Nagpur - 440 013
Ph. : 0712-2580011 Fax : 0712 - 2583237
ISO 9001 : 2008 CERTIFIED ORGANISATION

About the Department :
Department of Electronics Engineering was established in 1986. The National Board of Accreditation, New Delhi has accredited the department thrice in succession in the year 2003, 2007 & 2013. The Department offers a Post Graduate programme in M. Tech. (VLSI Design). It is recognized centre for M.E. (by Research) and Doctoral programmes of RTM Nagpur University. The department has received a grant of Rs. 10 lakhs from AICTE under its MODROB scheme to carry out projects in CMOS VLSI area. The Department has 15 state of the art laboratories with investment over Rs. 2 Crores. The major softwares include VLSI design, development and verification platforms, such as Mentor Graphics FPGA advantage, Agilent ADS, digital design simulation, synthesis tool and Synopsys's analog/digital tool set. The backend place and route vendor specific tools are Xilinx's ISE Development Platform, Altera's NIOS II Development Platform, Tanner tool, ORCAD 15.7. The design Platforms include virtex 5 Development platform and Embedded System Design environment like NIOS II, Embedded Evaluation CYCLONE III Platform, ARM Development Platform. Advanced Communication trainers and test equipments include Fiber Optic Trainer, Spectrum Analyzer, Digital Storage Oscilloscope, MIC Trainer, Digital Signal Processors simulation tools, MATLAB, LABVIEW are part of the state-of-the- art laboratories.

About the Programme :
The post graduate curriculum is well designed to expose the students to design complexities of contemporary Digital/ Mixed Signal and Embedded systems using industry standard EDA tools and development platforms. In order to prepare post graduates to take gainful employment in core, allied sector of electronics engineering and entrepreneurship, the curriculum components include hands-on training, core-elective courses and industry oriented projects. Students undergo major projects with joint academic and research collaboration under Indian Nano-electronics Users Program (INUP) at IIT Bombay, IIT Gandhinagar, ISRO, Godrej and NEERI.

Vision of Department:
Electronics Engineering Department endeavors to facilitate state of the art technical education in the field of electronics engineering by infusing scientific temper in the students leading towards research and to grow as centre of excellence in the field of microelectronics.

Mission of Department:
- To promote quality education through stimulating environment for dissemination of knowledge and technology.
- To impart necessary technical, professional skills with moral and ethical values to enable students for achieving a successful career.
- To develop centre of excellence in the field of microelectronics and its allied areas with continuing education program.
- To foster research and development in collaboration with institutions/industries.

Program Objectives :
1. To develop professionals with an ability to analyze and design digital, analog / mixed signal and Embedded Systems.
2. To develop necessary skills to enable graduates to assume position of technical and / or managerial leadership in their career.
3. To encourage life-long learning with commitment to ethical practices

Program Outcomes:
a) An ability to apply knowledge of mathematics, science, and engineeringfundamentals appropriate to the discipline.
b) An ability to design and implement systems by critically analyzing and interpreting design specifications with appropriate consideration for society, finance and environment.
c) An ability to function individually and in groups, including diverseand multidisciplinary fields, to accomplish a common goal.
d) An ability to identify, formulate and solve problems pertaining to discipline.
e) An understanding of professional and ethical responsibility.
f) An ability to communicate effectively.
g) An ability to engage in self, reflective, life-long learning in continuing professional development.
h) Knowledge of contemporary issues.
i) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practices.
j) An understanding of engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects.
k) An ability to apply appropriate research methodologies and contribute towards development of scientific knowledge in engineering discipline.

SCHEME OF EXAMINATION OF M. TECH (VLSI DESIGN)
SEMESTER PATTERN

I SEMESTER M. TECH (VLSI DESIGN)

Sr. No.	Code	Course	L	T	P	Credits	Maximum Marks			Exam Duration
							Internal Assessment	End Sem Exam	Total	
1	ENT501	CMOS Digital Circuit Design	4	0	0	8	40	60	100	3 Hrs.
2	ENP501	CMOS Digital Circuit Design Lab.	0	0	2	2	25	25	50	3 Hrs.
3	ENT502	Digital System Design and Synthesis	3	0	0	6	40	60	100	3 Hrs.
4	ENP502	Digital System Design and Synthesis Lab.	0	0	2	2	25	25	50	3 Hrs.
5	ENT503	VLSI Technology	4	0	0	8	40	60	100	3 Hrs.
6	ENT504	Physical Electronics & Circuit Simulation	4	0	0	8	40	60	100	3 Hrs.
7	ENP504	Physical Electronics & Circuit Simulation Lab.	0	0	2	2	25	25	50	3 Hrs.
8	ENT505	Advanced Processors for Embedded System	3	0	0	6	40	60	100	3 Hrs.
9	ENP505	Advanced Processors for Embedded System Lab.	0	0	2	2	25	25	50	3 Hrs.
		Total	18	0	8	44				

SCHEME OF EXAMINATION OF M. TECH (VLSI DESIGN)
SEMESTER PATTERN

II SEMESTER M. TECH (VLSI DESIGN)

Sr. No.	Code	Course	L	T	P	Credits	Maximum Marks			Exam Duration
							Internal Assessment	End Sem Exam	Total	
1	ENT506	Analog IC Design	3	0	0	6	40	60	100	3 Hrs.
2	ENP506	Analog IC DesignLab.	0	0	2	2	25	25	50	3 Hrs.
3	ENT507	Digital System Design and Verification.	4	0	0	8	40	60	100	3 Hrs.
4	ENP507	Digital System Design and Verification Lab.	0	0	2	2	25	25	50	3 Hrs.
5	ENT508	Advanced Topics in Signal Processing	3	0	0	6	40	60	100	3 Hrs.
6	ENP508	Advanced Topics in Signal Processing Lab.	0	0	2	2	25	25	50	3 Hrs.
7	ENT509	RF Circuit Design	3	0	0	6	40	60	100	3 Hrs.
8	ENP509	RF Circuit DesignLab.	0	0	2	2	25	25	50	3 Hrs.
9	ENT510	Elective I	4	0	0	8	40	60	100	3 Hrs.
		Total	17	0	8	42				

Course Code	Elective I
ENT510-1	Memory Design and Testing
ENT510-2	VLSI Signal Processing
ENT510-4	Micro-Sensors and MEMS

SCHEME OF EXAMINATION OF M. TECH (VLSI DESIGN)
SEMESTER PATTERN

III SEMESTER M. TECH (VLSI DESIGN)

Sr. No.	Code	Course	L	T	P	Credits	Maximum Marks			Exam Duration
							Internal Assessment	End Sem Exam	Total	
1	ENT601	Research Methodology	3	0	0	6	40	60	100	3 Hrs.
2	ENT602	Elective -II	4	0	0	8	40	60	100	3 Hrs.
3	ENT603	Elective -III	4	0	0	8	40	60	100	3 Hrs.
4	ENP604	Project Phase I	0	0	6	24	100	100	200	---
		Total	11	0	6	46				

Course Code	Elective II	Course Code	Elective III
ENT602-1	Adv. Computer Architecture	ENT603-1	VLSI Testing
ENT602-4	Nanoelectronics	ENT603-2	Wireless Digital Communication
ENT602-3	Low Power VLSI design	ENT603-3	Advanced Embedded Systems

SCHEME OF EXAMINATION OF M. TECH (VLSI DESIGN)
SEMESTER PATTERN

IV SEMESTER M. TECH (VLSI DESIGN)

Sr. No.	Code	Course	L	T	P	Credits	Maximum Marks			Exam Duration
							Internal Assessment	End Sem Exam	Total	
1	ENP605	Dissertation / Thesis (Viva-Voce)	0	0	12	48	200	200	400	
		Total	0	0	12	48				

SYLLABUS OF SEMESTER I, M.TECH. (VLSI DESIGN)

Course Code : ENT501 **Course : CMOS Digital Circuit Design**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 8**

Course Objectives :

The objective of this course is to provide students with

1. knowledge of circuit models for analysis of digital CMOS circuits and interconnect .
2. implementation technique necessary to realize CMOS circuits/ Sub-systems using various CMOS logic structures.
3. computation methods required for circuit characterization and performance estimation.
4. understanding of various CMOS processes and emerging nanometer-scale technologies.

Course Outcomes :

Upon completion of this course, students should demonstrate the ability to :

I. apply the circuit models to investigate CMOS circuits.
II. design moderately sized CMOS circuits/ sub-systems and compute timing, power and parasitic for various CMOS Logic structures.
III. evaluate various micron, deep sub micron and nanometer-scale technologies.

Syllabus

Introduction to MOS Transistors, Switches, CMOS Logic, Scaling and transistors structures for VLSI; Silicon-on-insulator transistors.

Static Load MOS Inverters, CMOS Inverter, the Tri State Inverter.

Circuit Characterization and Performance Estimation: Introduction, Resistance Estimation Capacitance Estimation, Switching Characteristics, Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing.

CMOS Circuit And Logic Design: CMOS Logic Gate Design, CMOS Logic Structures, Clocking Strategies, I/O Structures, Driving Large capacitive loads.

CMOS Sub System Design: Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Binary Counters, ALUs, Multiplication, Shifters, Memory Elements, Control-FSM, Control Logic Implementation.

Memory elements: Read write memory, RAM, Register files, FIFO, LIFO, SIPO, Serial access Memory, CAM, ROM.

Text books :

1. Digital Integrated Circuits: A Design Perspective: J. Rabaey, A Chandrakasan, B Nikolic, PHI
2. Principles of CMOS VLSI Design : N. Weste and K. Eshraghian, Second edition, Person
3. Basic VLSI Design : Systems and circuits, D. Pucknell, K. Eshraghian, PHI

Reference books:

1. CMOS Digital Integrated Circuits Analysis & Design: S M Kang, Yusuf Lablebici, TMH
2. VLSI Design Techniques for Analog and Digital Circuits, Randall & Geiger, McGrow Hill
3. Introduction to VLSI System : Carver Mead, Lynn Conway, Addison-Wesley

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENP501 **Course : CMOS Digital Circuit Design Lab**

L : 0 Hrs., P : 2 Hrs., Per week **Credits : 2**

Practicals/ Case Studies/ Mini projects based on syllabus of ENT501

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENT502 **Course : Digital System Design and Synthesis**

L : 3 Hrs., P : 0 Hrs., Per week **Credits : 6**

Course Objective :

The objective of this course is to provide students with

1. knowledge of complete digital system design flow.
2. language constructs of VHDL and its different modeling styles for system design.
3. concepts of test benches, text I/O, synthesis process, timing analysis and related issues.
4. design essentials of Finite State Machine / Asynchronous State Machine
5. knowledge of various programmable device architecture

Course Outcomes :

Upon the completion of this course, students will demonstrate the ability to:

I. describe the digital system design flow
II. design the digital systems in VHDL using different modeling styles.
III. test and analyze the digital systems using test bench and text I/O.
IV. optimize the digital systems in terms of area, timing and power.
V. implement the digital system on various programmable devices.

Syllabus

Concepts of Digital System Design : The role of hardware description languages (HDL) in state-of-the-art methodologies of digital systems design, Multi-level approach to digital systems design, The design flow of digital systems.

Concepts of hardware description languages : Event/cycle driven simulators, Syntax and Semantics of VHDL, Data objects, data types, arrays and attributes, Operators, expressions and signal assignments, Concurrent and sequential constructs, Procedures and functions, Examples of design using VHDL, Modeling a test bench, Text IO handling.

Synthesis : Stages of synthesis, Synthesis inputs, Logic described by RTL, Synthesizable subset of RTL, Latches and flip flops using RTL, Declaration for a generic netlist, Technology mapping

Synthesis-Analysis: Static timing analysis, Synthesis constraint, Timing exceptions, Register synthesis timing constraints, Timing summary report, Logic partitioning and timing budgeting,

Constraining a design, Gate level simulation.Synthesizing FSM, synchronous FSM designs, ASM Design.

Programmable logic Devices: ROM, PLA, PAL PLD- Features, programming and applications using complex programmable logic devices.

FPGA technologies: Anti fuse, static RAM - EPROM and EEPROM technology. Xilinx LCA - Altera FLEX, Xilinx I/O blocks, Study of block RAM's, Clock Managers-Resources of FPGA, Introduction to Xilinx's Spartan &Virtex FPGAs architecture & Altera Cyclone Architecture.

Text books :

1. VHDL Primer: J. Bhasker, Pearson Education
2. The Design Warrior's Guide to FPGAs-Devices, Tools and Flows: Clive Maxfield, Elsevier
3. VHDL Synthesis: J. Bhasker, Star galaxy
4. Synthesis and optimization of digital circuits :Giovanni De Micheli, McGraw-Hill
5. Logic synthesis and verification algorithms: Gary D. Hachtel, Fabio Somenzi, Springer.

Reference books:

1. Digital Electronics And Design With VHDL, 1st ed.: A. Pedroni, Volnet Elsevier
2. Digital Systems Design Using VHDL Thomson Learning: Charles H. Roth. Jr., Inc.
3. Spartan-3 Generation FPGA User Guide, UG331 (v1.7)
4. Cyclone II Device Handbook, Volume 1
5. An Engineering Approach to Digital Design: W. Fletcher. Prentice Hall

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENP502 **Course : Digital System Design and Synthesis Lab.**

L : 0 Hrs., P : 2 Hrs., Per week **Credits : 2**

Practicals/ Case Studies/ Mini projects based on syllabus of ENT502

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENT503 **Course : VLSI Technology**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 8**

Course Objectives :

The objective of this course is to provide students with

1. knowledge of the scientific principles involved in fabrication of integrated circuits.
2. understanding of fabrication steps involved in fabrication process of MOSFET.
3. a comprehensive understanding of process integration and manufacturing for integrated circuits.

Course outcomes :

Upon the completion of this course, students will demonstrate the ability to:

I. plan a sequence of processing steps to fabricate a solid state device to meet geometric, electrical, and/or processing parameters.
II. design VLSI circuits by keeping technological process constraints in mind.
III. understand the relevance of a process or device, either proposed, past or existing, to current manufacturing practices.

Syllabus

Environment for VLSI Technology : Clean room and safety requirements, Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation : Solid State diffusion modeling and technology; Ion Implantation modeling, technology and damage annealing; characterization of impurity profiles.

Oxidation : Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films, Oxidation technologies in VLSI and ULSI; Characterization of oxide films, High k and low k dielectrics for ULSI.

Lithography : Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

Chemical Vapor Deposition techniques : CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modeling and technology.

Metal film deposition : Evaporation and sputtering techniques, Failure mechanisms in metal interconnects; Multi-level metallization schemes.

Plasma and Rapid Thermal Processing : PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.

Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technologies.

Text Books :

1. ULSI Technology: C. Y. Chang and S. M. Sze (Ed), McGraw Hill Companies Inc, (1996).
2. VLSI Fabrication Principles: S. K. Ghandhi, John Wiley Inc., New York, (1983).
3. VLSI Technology 2nd ed.: S. M. Sze (Ed), McGraw Hill, (1988).

Reference Books:

1. Physics of Semiconductor Devices: S. M. Sze, Wiley Eastern, (1981).

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENT504 **Course : Physical Electronics & Circuit simulation**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 8**

Course Objective :

The objective of this course is to provide students with

1. essentials of semiconductor physics to mathematically analyze PN junctions, and MOSFETs.
2. understanding of various semiconductor device models and parameters.
3. knowledge of computer simulation for circuits.

Course Outcomes :

Upon the completion of this course, students will demonstrate the ability to:

I. apply the basic semiconductor physics concepts to better understand current and future devices.
II. analyze various semiconductor device models and parameters
III. perform device simulation using EDA tools to illustrate and explore device behavior

Syllabus

Introduction to semiconductor Physics: Electrons in periodic lattices, E-k diagrams, electrons, holes and phonons. Boltzmann transport equation, mobility and diffusivity; Carrier statistics; Continuity equation, Poisson's equation

Semiconductor junctions: Schottky, homo- and hetero-junction band diagrams and I-V characteristics.

MOS structures : The ideal and non ideal MOS capacitor band diagrams and CVs; Effects of oxide charges, defects and interface states; Characterization of MOS capacitors: HF and LF CVs, avalanche injection; High field effects and breakdown.

The MOS transistor : Pao-Sah and Brews models; Short channel effects in MOS transistors. High-field and radiation effects in transistors, Scaling.

Device modeling, MOS Models, BSIM Spice models, Circuit simulation using Spice.

Text Books:

1. Analysis and Design of Analog ICs 3rd ed.: Paul, Grey, and R Mear, J Willy and Sons, USA (1993).
2. VLSI Design techniques for Analog and Digital Circuits: R.L. Geiger, P.E. Allen, McGraw Hill
3. Design of Analog CMOS Integrated circuits : B Razavi, Tata Mcgrw Hill

Reference Books:

1. CMOS Analog Circuit Design: Allan Holberg, OUP, Second Edition.
2. CMOS Circuit Design, Layout and simulation: J. Baker, D.E. Boyce., IEEE press.
3. Fundamental of Micro-electronics: BehzadRazavi, Preview edition, Wiley Press.

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENP504 **Course : Physical Electronics & Circuit simulation Lab.**

L : 0 Hrs., P : 2 Hrs., Per week **Credits : 2**

Practicals / Case Studies / Mini projects based on syllabus of ENT504

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: ENT505 **Course: Advanced Processors for Embedded System**

L : 3 Hrs., P : 0 Hrs., Per week **Credits : 6**

Course Objective :

The objective of this course is to provide students with

1. understanding of RISC principles and RISC processor architectures.
2. deep understanding of ARM architecture and its organization.
3. programming concepts of ARM based microcontroller.
4. fundamentals of operating system for Embedded System.

Course Outcomes :

Upon the completion of this course, students will demonstrate the ability to:

I. applythe knowledge of ARM architecture and organization for modern ARM devices.
II. utilize knowledge, techniques and skill to integrate microcontroller hardware and software
III. use the concepts of Embedded operating System for designing OS based application.

Syllabus

Introduction to embedded systems, Concept, Embedded System Design Issues.

RISC Principles, MIPS Architecture, SPARC Architecture, PowerPC Architecture, Itanium Architecture, ARM Architecture.

ARM Processor Fundamentals : Current Program Status Register, Pipeline, Exceptions Interrupts, and the Vector Table Core Extensions , Architecture Revisions, ARM Processor Families

Introduction to the ARM Instruction Set, Introduction to the Thumb Instruction Set.

ARM: Exception and Interrupt Handling, Assembly Language Programming and interfacing.

Introduction to Operating system for Embedded System.

Text Books:

1. ARM System Developer's Guide Designing and Optimizing System Software: Andrew N. Sloss, Dominic Symes, Chris Wright, Morgan Kaufmann publications.
2. ARM system on chip Architecture: Steve Furber, Person Education.

Reference Books:

1. Guide to RISC Processors for Programmers and Engineers: Sivarama P. Dandamudi, Springer
2. Embedded System Design: Steve Heath, Butterworth Helnemann.
3. Micro C/OS II The Real Time Kernel: Jean J. Labrosse

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENP505 **Course : Advanced Processors for Embedded System Lab.**

L : 0 Hrs., P : 2 Hrs., Per week **Credits : 2**

Practicals/ Case Studies/ Mini projects based on syllabus of ENT505

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENT506 **Course : Analog IC Design**

L : 3 Hrs., P : 0 Hrs., Per week **Credits : 6**

Course Objectives:

The objective of this course is to provide students with

1. sound understanding of metal-oxide-semiconductor field-effect transistor and the relationship of process technology with models used for analog IC.
2. analysis, up to and including second-order effects caused by scaling of CMOS technology and modeling deficiencies.
3. techniques for analyzing and designing a variety of analog circuits in CMOS technology.

Course Outcomes :

Upon the completion of this course, students will demonstrate the ability to:

I. use mathematical models of MOS transistors to evaluate their behavior in analog circuits.
II. select suitable design approaches while trading off conflicting requirements.
III. investigate various analog IC performance parameters.

Syllabus

Introduction to analog VLSI and mixed signal issues in CMOS technologies

Basic Building Blocks for IC : Switches. Current sources and sinks, Current mirrors, Bandgap references.

Amplifiers : MOS amplifiers, Common Source, Source follower, Common Gate and Cascode amplifiers. Frequency Response.

Differential Amplifier-Basic differential Pair, common mode response, Differential Pair with MOS loads, OPAMP Design, one-stage OPAMP, Two Stage OP-Amps.

Switch Capacitor circuits : General considerations, sampling switches, Switched capacitor integrator.

Data Converter Fundamentals, DAC/ADC Specifications, Data Converter Architectures: DAC architectures-Resistor String, Charge-Scaling DACs, Cyclic DAC, Pipeline DAC.

ADC Architectures-Flash, The Two-Step Flash ADC, The Pipeline ADC, Integrating ADCs, The Successive Approximation ADC.

Text Books:

1. Design of Analog CMOS IC: B Razavi, Tata Mcgrw Hill
2. CMOS Circuit Design, Layout and simulation: J. Baker, D.E. Boyce., IEEE press.
1. CMOS Analog Circuit Design: Allan Holberg, OUP, Second Edition.

Reference Books:

1. VLSI Design techniques for Analog and digital Circuits: R.L. Geiger, P.E. Allen, McGraw Hill
2. Analysis And Design Of Analog ICs 3rd ed.: Paul, Grey, and R Mear, J Willy and Sons, USA.
3. IEEE Journal of Solid state Circuits

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENP506 **Course : Analog IC DesignLab.**

L : 0 Hrs., P : 2 Hrs., Per week **Credits : 2**

Practicals / Case Studies / Mini projects based on syllabus of ENT506

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENT507 **Course : Digital System Design and Verification**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 8**

Course Objective :

The objective of this course is to provide students with

1. language constructs of Verilog HDL and different modeling styles for system design.
2. fundamental of verification techniques.
3. insight of various attributes of System Verilog.

Course Outcome:

Upon the completion of this course, students will demonstrate the ability to:

I. implement digital Systems using Verilog HDL.
II. apply verification techniques to meet the specified requirements
III. use system Verilog to design, test and verify the digital systems

Syllabus

Modeling concepts with Verilog HDL.Levels of abstraction. Design methodologies. Comparison of sequential and parallel blocks.Basic compiler directives.Behavioral modeling. Behavioral modeling blocks, Procedural assignments: blocking and non-blocking. Data flow modeling. Assign statements. Delays.. Logic statement implementation.The conditional operator.Design examples using Verilog HDL.

Verification of digital systems using HDLs. Functional verification.Timing verification.Formal verification. Basics of equivalence checking and model checking.

Attributes of System Verilog.Data types.Array reduction methods. New type creation. Statements. Procedural, continue and break statements. Tasks and functions.Routine arguments Time unit and precision. Object Oriented Programming (OOP) terminology. Classes.Class instantiation.Compilation order.Verification environment.Ports.Interfaces.Communication with ports. Grouping signals. Benefits of interface usage.Clocking Blocks. Assertions. Assertion Types: procedural, immediate and strobed assertions. System Functions.Randomization.

Text Books :

1. Verilog HDL, 2/E: Samir Palnitkar, Publisher: Prentice Hall
2. Verilog Digital system Design: Navabi, McGraw Hill, (1999)
3. A Guide to Using SystemVerilog for Hardware Design and Modeling: Stuart Sutherland, Simon Davidmann, Peter Flake, Springer.
4. Advanced Digital Design with the Verilog HDL: M.D. Ciletti, (Prentice Hall), 2003. ISBN 0-13-089161-4.

Reference Books :

1. Verilog 2001: Stuart Sutherland, Kluwer (2002).
2. The Verilog PLI Handbook: Surherland, Kluwer. (1999).
3. Programmable Logic Devices Data book and Design Guide: National Semiconductors
4. Fault-Tolerant-Theory and Techniques. Vol and II: Pradnan D.K., Prentice Hall.
5. Digital Logic Circuit Analysis and Design: Nelson, Nagale, Carroil, Irwin, Prentice Hall

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENP507 **Course : Digital System Design and Verification Lab.**

L : 0 Hrs., P : 2 Hrs., Per week **Credits : 2**

Practicals/ Case Studies/ Mini projects based on syllabus of ENT507

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENT508 **Course : Advanced Topics in Signal Processing**

L : 3 Hrs., P : 0 Hrs., Per week **Credits : 6**

Course Objectives:

The objective of this course is to provide students with

1. fundamentals of multirate signal processing.
2. knowledgeof digital filters for multirate systems.
3. understanding of Digital Signal processor Architecture.
4. insightof the basic theory, algorithms and transforms used in digital image processing.

Course Outcome:

Upon the completion of this course, students will demonstrate the ability to:

I. analyze and design efficient multirate systems.
II. develop Digital Signal processor based application.
III. realize various algorithms of Digital image processing.
IV. develop critical thinking about shortcoming of the state of the art in image processing

Syllabus

Basics of signal Processing, Multirate Signal Processing: analysis of multirate structures, multistage design of decimator and interpolator, computationally efficient interpolator and decimator structures, Design of linear phase/poly-phase FIR filters.

Applications of Digital Signal Processing: Speech processing, sub-band coding, Digital Filter banks, Channel vocoder, Homomorphic Vocoder.

Digital signal processors : Overview, Architecture and Applications.

Elements of image processing system, applications, Intensity transformations and spatial filtering, Frequency Domain image transforms, 2D-DFT, 2D-DCT, Hadamard transform, Haar Transform, hotelling Transform, Fundamentals of wavelet transforms.

Image Segmentation: Region Based approach, Segmentation based on thresholding, Edge detection, Hough Transform.

Text Books:

1. Digital Signal Processing - A Computer Based Approach, 3rd ed.: Sanjit K. Mitra , TMH
2. Digital Image Processing (Second Edition): Gonzalez, R. C. woods, R. E.;Pearson Education.
3. Digital signal Processing - Principles, Algorithms and application 3rd ed.: Proakies, J. G.; Monolakis, D. G.: Prentice-Hall of India

Reference Books:

1. Fundamentals of Digital Image Processing: Jain, A. K. Prentice-Hall of India
2. Discrete time Signal Processing: Oppenheim A. V., Schaefer R.W. Prentice-Hall India
3. Digital Image Processing:Dr. S. Jayaraman, S. Esakkirajan, T. Veerakumar; Publisher: TMH

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENP508 **Course : Advanced Topics in Signal Processing Lab.**

L : 0 Hrs., P : 2 Hrs., Per week **Credits : 2**

Practicals/ Case Studies/ Mini projects based on syllabus of ENT508

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: ENT509 **Course : RF Circuit Design**

L : 3 Hrs., P : 0 Hrs., Per week **Credits : 6**

Course Objective :

The objective of this course is to provide students with

1. understanding of modern RF electronics devices employed in RF Transceiver Design
2. knowledge of various issues encountered in high-frequency circuits, such as impedance matching, realization of passive components and bandwidth enhancement.
3. knowledge to design components of radio-frequency systems, including low noise amplifiers, oscillators, mixers and power amplifiers.
4. understanding the effect of individual components performance on overall radio-frequency transmitter and receiver design and performance.

Course Outcomes :

Upon the completion of this course, students will demonstrate the ability to:

I. understand the architectures ,operation and performance specifications, tradeoff of a RF receiver and its building blocks.
II. design and analyze various building blocks of receiver like filters, LNA, Mixer, Power Amplifiers , VCO as per the specifications.
III. understand the sources of nonlinearity , noise, process technology and its impact on the performance parameters of individual blocks of receiver and on receiver performance.

Syllabus

Characteristics of passive components for RF circuits. Passive RLC networks.Transmission lines.Two-port network modeling. S-parameter model.The Smith Chart and its applications.

Active devices for RF circuits: SiGe MOSFET, GaAspHEMT, HBT and MESFET. PIN diode. Device parameters and their impact on circuit performance.

Review of analog filter design: Low-pass, high-pass, band-pass and band-reject filters.

RF Amplifier design, single and multi-stage amplifiers.

Low Noise Amplifier design: noise types and their characterization, LNA topologies, power match vs noise match. Linearity and large-signal performance.

RF Power amplifiers: General properties. Class A, B, AB, C, D, E and F amplifiers. Modulation of power amplifiers.

Analog communication circuits: Mixers, phase-locked loops, oscillators, Transceiver performance specification.

Text Books:

1. The Design of CMOS Radio Frequency Integrated Circuits: Thomas H. Lee- Cambridge University Press.
2. RF Circuit Design Theory & Applications : Reinhold Ludwing - Pearson Education

Reference Books:

1. RF Microelectronics : Behzad Razavi : Pearson Education
2. VLSI for wireless communication: Bosco Leung- Pearson Education

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENP509 **Course : RF Circuit Design Lab.**

L : 0 Hrs., P : 2 Hrs., Per week **Credits : 2**

Practicals/ Case Studies/ Mini projects based on syllabus of ENT509

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENT510-1 **Course : Memory Design and Testing**

L : 4 Hrs., P : 0 Hrs., Per week **Credits: 8**

Course Objective:

The objective of this course is to provide students with

1. Comprehensive understanding of Static Random Access Memory (SRAMs), Dynamic Random Access Memory (DRAM) and Nonvolatile Memory Architectures and their feature comparison
2. Understanding Memory Fault Modeling, Testing, and Memory Design for Testability.

Course Outcome :

Upon the completion of this course, students will demonstrate the ability to:

I. Apprehend SRAM, DRAM and Nonvolatile Memory Architectures
II. Understand Memory Fault Modeling, Testing, and Memory Design for Testability.
III. Understand design trade-off in Memory design.

Random Access Memory Technologies

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.

Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

Nonvolatile Memories : Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One- Time Programmable (OTP) EPROMS-Electrically Erasable PROMs (EEPROMs)- EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

Memory Fault Modeling, Testing, And Memory Design For Testability And Fault Tolerance RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

Advanced Memory Technologies And High-Density Memory Packaging Technologies Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs- Analog Memories-Magnetoresistive Random Access Memories (MRAMs)

Text Books:

1. Semiconductor Memories Technology, Testing and Reliability: A. K. Sharma, IEEE Press.
2. Semiconductor Memory design & application: Luecke Mize Care, McGraw Hill.
3. Semiconductor Memory Design Handbook: Belty Prince

Reference Books:

1. Memory Technology design and testing 1999 IEEE International Workshop on: IEEE Computer Society Sponsor (S)

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENT510-2 **Course : VLSI Signal Processing**

L : 4 Hrs., P : 0 Hrs., Per week **Credits: 8**

Course Objective :

The objective of this course is to provide students with

1. conceptsof pipelining, parallel processing, retiming, folding and unfolding for digital signal processing architectures.
2. knowledge of systolic architecture
3. analysis to optimize fast convolution algorithms for digital signal processing architectures in terms of computational complexity.

Course Outcome :

Upon the completion of this course, students will demonstrate the ability to:

I. apply the concepts of pipelining, parallel processing, Retiming, Folding and unfolding to optimize digital signal processing architectures .
II. analyze data flow in systolic architectures.
III. minimize the computational complexity using fast convolution algorithms.

Syllabus

Pipeling and Parallel Processing: introduction, pipeling of FIR Digital filters Parallel processing. Pipelining and parallel processing for low power.

Retiming: Introduction, Definition and properties, Solving system of inequalities, retiming techniques.

Unfolding Introduction An algorithms for unfolding, Properties of unfolding, Critical path, unfolding and retiming Application of unfolding.

Folding : Introduction Folding Transformation, Register Minimization Techniques, Register minimization in folded architectures Folding if Multirate systems

Systolic Architecture Design : Introduction, Systolic Array Design Methodology, FIR systolic Arrays, Selection of scheduling vector, Matrix Multiplication and 2D systolic array Design, Systolic design for space representations containing Delays.

Fast Convolution: Introduction, Cook, Toom algorithm, Winogard algorithm, iterated convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

Text Books :

1. VLSI Digital Signal Processing Systems: Keshab K. Parhi. Wiley-Inter Sciences. (1999).
2. Analog VLSI signal and information processing: Mohammed Ismail, Terri, Fiez, McGraw Hill. (1994).
3. VLSI Digital signal processing system Design and implementation: Keshab. Parthi, Wiley-Inter science, (1999).

Reference Books:

1. VLSI and Modern singal processing: kung. S. Y., H. J. While house T. Kailath, prentice hall, (1985).
   Design of Analog Digital VLSI circuits for telecommunications and signal processing :Jose E. France, YannisTsividls, prentice Hall, (1994).

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENT510-4 **Course : Micro-Sensors and MEMS**

L : 4 Hrs., P : 0 Hrs., Per week **Total Credits : 8**

Course Objectives :

The objective of this course is to provide students with

1. fundamental understanding of standard microfabrication techniques
2. understanding of working principles of microsensors, actuators used in microsystems.
3. major classes, components, and applications of MEMS devices/systems

Course Outcomes :

Upon the completion of this course, students will demonstrate the ability to

I. apply the principles behind the operation of MEMS devices
II. choose a micromachining technique for a specific MEMS fabrication process
III. design and fabricate MEMS devices or a microsystem
IV. understand recent advancements in the field of MEMS and devices.

Syllabus

Microfabrication and Micromachining : Integrated Circuit Processes, Bulk Micromachining : Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA)

Physical Microsensors : Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors

Microactuators : Electromagnetic and Thermal microactuation, Mechanical design of microactuators, Microactuator examples, microvalves, micropumps, micromotors-Microactuator systems : Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector

Surface Micromachining : One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micromachined Systems : Success Stories, Micromotors, Gear trains, Mechanisms

Application Areas : All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays.

MEMS for RF Applications : Need for RF MEMS components in communications, space and defense applications.

Text Books :

1. Sensor Technology and Devices: Ristic L (ed), Artech House, London, 1994.
2. Semiconductor Sensors: Sze S.M. (ed), John Wiley, New York, 1994.
3. RF MEMS and Their Applications: Vijay Varadan, K. J. Vinoy, K. A. Jose, Wiley, 2002.

Reference Books :

1. Integrated Sensors, Micro actuators and micro-systems (MEMS): K.D. Wise, Special Issue of proceedings of IEEE, Vol. 86, No.8, August 1998
2. RF MEMS: Theory, Design, and Technology: Gabriel M. Rebeiz, Wiley, 2003.
3. Fundamentals of Microfabrication :Marc Madou, CRC Press, 1997.

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code : ENT601 **Course :RESEARCH METHODOLOGY**

L : 3 Hrs., P : 0 Hrs., Per week **Credits : 6**

Course Objectives:

The objective of this course is to provide students with

1. an insight into how scientific research is conducted
2. knowledge of Research Process, Concepts, diverse research tasks and equip them to undertake research.
3. understanding the concepts of Data collection, system modeling and reliability.
4. methods for presentation of research results.

Course Outcome :

Upon the completion of this course, students will demonstrate the ability to:

I. evaluate current research and propose possible alternate directions for further work.
II. develop hypothesis and methodology for research
III. comprehend and deal with complex research issues in order to communicate their scientific results clearly for peer review.

Syllabus

Research: Research Process, Research Concept and demonstration of different types of research task

Research design and hypothesis: Problem identification and formulation, hypothesis types and verification, methods of research.

Data collection and Modeling: Literature review, data analysis, Logic / Experimental / Field data based modeling, modeling based on design of new system/ Process/ Product, Modeling based on Statistical Concepts.

System modeling: Simulation modeling, verification and validation of model, Validation of results, optimization of model and case studies.

Reliability of Established Model: Review of theory of reliability,Hazard models, System Reliability

Report writing and outcome: Structure and contents of report, presentation of findings, formats of report writing, formats of publication in research journals, Referencing in academic writing,Ethics in research, electronic and internet sources, Intellectual Property.

Reference Books :

1. Angela Dean and Daniel Voss, Design and Analysis of Experiments, Published by Springer-Verlag New York, In
2. H. Schenck Jr., Theories of Engineering Experimentation, Mc-Graw Hill, First Edition
3. Law, A. M., and W. D. Kelton, 1991, Simulation Modeling and Analysis, Second Edition, McGraw-Hill
4. Banks, J.J., S. Carson, and B. L. Nelson. 1996. Discrete event system simulation. 2d ed. Upper saddle river, New Jersey: Prentice-Hall.

5. Montgomery, Douglas C. (2007), 5/e, Design and Analysis of Experiments, (Wiley India)
6. Montgomery, Douglas C. &Runger, George C. (2007), 3/e, Applied Statistics & Probability for Engineers (Wiley India)
7. Kothari C.K. (2004), 2/e, Research Methodology- Methods and Techniques (New Age International, New Delhi)
8. Srinath L. S., Reliability Engineering East West Press (EWP)

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code : ENT602-1 **Course : Advanced Computer Architecture**

L : 4 Hrs., P : 0 Hrs., Per week **Total Credits : 8**

Course Objectives

The objective of this course is to provide students with

- Understanding advanced computer architecture aspects
- Understanding Models of parallel computer and conditions for parallelism
- Understanding Multiprocessors and multi-computer aspects
- Understanding advanced processor technology
- An ability to design pipelined processors

Course Outcomes

Upon the completion of this course, student will demonstrate the ability to:

- Describe the principles of computer design.
- Describe the operation of performance enhancements such as pipelines, caches and vector processors.
- Describe the cache and shared memory organization.
- Describe modern architectures such as RISC, Super Scalar, VLIW.
- Compare the performance of different architectures.
- Improve application performance for different CPU architectures.
- Develop applications for high performance computing systems.

Models of parallel computer, multiprocessors and multicomputers, multivector and SIMP computers, PRAM and VLSI model, conditions of parallelism, data and resource dependencies, grain size and latency, grain packing and scheduling , program flow mechanisms, system interconnect architectures.

Principles of scalable performance, performance metrics and measures, speedup performance laws, advanced processor technology, superscalar and vector processors, cache memory organizations, shared memory organizations.

Pipeline and superscalar techniques, linear pipeline processors, reservation and latency analysis, collision free scheduling, pipeline schedule optimization, instruction pipeline design, arithmetic pipeline design, superscalar and superpipeline design.

Multiprocessors and multi computers, multiprocessor system interconnects, cache coherence and synchronization mechanisms, message passing schemes.

Multivector and SIMD computers, vector processing principles, compound vector processing, SIMD computer organizations scalable multithreaded and dataflow architectures.

Elementary theory about dependence analysis, techniques for extraction of parallelism.

Text Books :

1. Advanced Computer Architecture: Kai Hwang; McGraw Hill.
2. Advanced Computer Architecture:Richard Y.Kausi ; Prentice Hall of India
3. Advanced Computer Architecture and Computing: S.S. Jadhav, Technical Publication, Pune

Reference Books:

1. Advanced Computer Architectures : A Design Space Approach : Dezso Sima, Terence Fountain, Péter Kacsuk, pearson Education

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code : ENT602-4 **Course : NANOELECTRONICS**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 8**

Course Objective :

1. To develop substantial understanding of contemporary relevance and potential of nanoelectronics;
2. To develop appreciation of how factors like scaling and dimension lead to novel behaviour of nanoelectronic components;
3. To develop understanding of the importance of quantum ideas and their place in modelling of nanoelectronic phenomena and devices;
4. To expose the student to a variety of nanoelectronic phenomena, nanoelectronic components and their possible applications.

Course Outcomes :

I. Students will show a deeper understanding of the relation between novel behaviour of nanoelectronic devices and quantum behaviour of matter at the nano scale as well as the breakdown of received scaling wisdom;
II. Students will appreciate scaling issues and ideas behind nanoscale fabrication technologies;
III. Students will have a working knowledge of fundamental concepts and methods of quantum mechanics as they are used in modelling of nanoelectronic devices;
IV. Students will understand concepts like quantum tunneling, resonant tunneling, Coulomb blockade, density of quantum states, quantum statistics and quantum modelling;
V. Students will have an understanding of principles of devices such as tunneling diodes, single electron transistor, spintronic devices

Syllabus

Shrink-down approaches : Introduction, CMOS Scaling, The nanoscale MOSFET, Finfets, Vertical MOSFETs, limits to scaling, system integration limits (interconnect issues etc.), Resonant Tunneling Transistors, Single electron transistors, new storage, optoelectronic, and spintronics devices.

Atoms-up approaches: Molecular electronics involving single molecules as electronic devices, transport in molecular structures, molecular systems as alternatives to conventional electronics, molecular interconnects; Carbon nanotube electronics, bandstructure and transport, devices, applications.

Text Books:

1. Fundamentals of Nanoelectronics: G.W.Hanson,Pearson Education.
2. Introduction to Nanotechnology: C.P. Poole Jr., F.J. Owens,Wiley (2003).
3. Nanoelectronics and Information Technology (Advanced Electronic Materials and Novel Devices): WaserRanier, Wiley-VCH (2003)

Reference Books:

1. Nanosystems: K.E. Drexler, Wiley (1992).
2. The Physics of Low-Dimensional Semiconductors: John H. Davies, Cambridge University Press, 1998.
3. Introduction to nanoelectronics: science, nanotechnology, engineering, and Applications: VladimirVasilevichMitin, ViacheslavAleksandrovichKochelap, Michael A. Stroscio,Cambridge.

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code : ENT602-3 **Course : LOW POWER VLSI DESIGN**

L : 4 Hrs., P : 0 Hrs., Per week **Total Credits : 8**

Course Objectives:

The objective of this course is to provide students with

1. Understanding of sources of power consumption of CMOS circuits
2. Understanding of Power Reduction Techniques and Low Power Logic design Styles.

Course Outcome:

Upon the completion of this course, students will demonstrate the ability to:

I. analyze the power consumption of CMOS circuits
II. design low-power CMOS circuits using various strategies at different design levels

Introduction : Advances in IC technologies. Design challenges in deep submicron MOS. Power dissipation. Power density. Supply voltage scaling. Scaling impact on supply current. Supply voltage scaling impact on delay. Power consumption and battery capacity trends.Power sources for low-power devices. Classes of batteries, battery types classification of application.

CMOS Power Consumtion Sources, Capacitance in a CMOS circuit, Dynamic Power Reduction Techniques: transition probability minimization, glitch reduction, supply voltage reduction, clock gating, multi-supply design, dynamic voltage and frequency scaling. Clock gating. Multi-supply design: multiple VDD considerations, optimum numbers of supplies, dual-supply inside a logic block, level shifters, distributing multiple supply voltage: conventional and shared-well.

Power Reduction Techniques : multiple threshold, transistor stacking, input vector control, sleep transistor, variable threshold technique.Multiple threshold technique, dual threshold CMOS, using multiple thresholds.Transistor stacking, self-reverse biasing, leakage control stacking.Input vector control: influence on subthreshold, gate, BTBT and total leakage.Sleep transistor technique. Low power sensor networks.

Low Power Logic Styles : Advantages and disadvantages of static CMOS. Low-power logic styles, Logic activity. Charge leakage. Problems with dynamic CMOS. Domino Logic.Selecting a logic style. Adiabatic Logic.Power saving and energy recovery. Charging with constant current, charge in N steps. Adiabatic dynamic CMOS inverter Quasi-Adiabatic Logic.Technology distribution.Power and area analysis.

Text Books :

1. Low Power Digital CMOS Design, 1 edition. Chandrakasan, R. Brodersen.Springer
2. Low-Power CMOS Circuits: Technology, Logic Design and CAD Tools: C. Piguet CRC.
3. Low-Power Digital VLSI Design: Circuits and Systems: A. Bellaouar, M. Elmasry.Springer; 1 edition.

Reference Books:

1. CMOS/BiCMOS VLSI: Low Voltage, Low Power :K.S. Yeo, S.S. Rofail, W.L. Goh, - Prentice Hall.
2. Low-Power CMOS VLSI Circuit Design: K. Roy, John Wiley & Sons Inc.

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code : ENT603-1 **Course : VLSI TESTING**

L : 4 Hrs., P : 0 Hrs., Per week **Total Credits : 8**

Course Objective:

The objective of this course is to provide students with

1. understanding of VLSI design testing issues.
2. concepts of fault modeling and simulation.
3. techniques to generate test patterns for faults in a system and design a system for testability.
4. knowledge of boundary scan standard and testing techniques for CMOS IC's.

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

I. identify the different testing issues.
II. apply knowledge of test-pattern generation and Design for testability techniques for testing of digital systems.
III. understand boundary scan standard and testing techniques for CMOS IC's.

Syllabus

Scope of testing and verification in VLSI design process.Issues in test and verification of complex chips, embedded cores and SOCs.

Fundamentals of VLSI testing. Fault models. Automatic test pattern generation.

Design for testability. Scan design. Test interface and boundary scan.

System testing and test for SOCs. Iddq testing. Delay fault testing. BIST for testing of logic and memories. Test automation, MCM testing.

Parametric testing, Reliability modeling, Yield models.

TextBooks :

1. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits: M. Bushnell and V. D. Agrawal, Kluwer Academic Publishers, 2000.
2. Digital Systems Testing and Testable Design: M. Abramovici, M. A. Breuer and A. D. Friedman, IEEE Press, 1990.

Reference Books:

1. Introduction to Formal Hardware Verification: T.Kropf, Springer Verlag, 2000.
2. System-on-a-Chip Verification-Methodology and Techniques: P. Rashinkar, Paterson and L. Singh, Kluwer Academic Publishers, 2001.

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code : ENT603-2 **Course : Wireless Digital Communication**

L : 4 Hrs., P : 0 Hrs., Per week **Total Credits : 8**

Course Objectives :

The objective of this course is to provide students with

1. The concept of cellular telephone system
2. Mobile radio environment, carrier synchronization & tracking methods and diversity
3. Different digital modulation and keying methodologies for mobile communication
4. Insight to different wireless communication systems

Course Outcome :

Upon the completion of this course, students will demonstrate the ability to:

1. Understand the concepts of cellular telephone system
2. Use tracking methods and diversity techniques to improve the performance of mobile communication system
3. Understand the concept of digital modulation, keying techniques and spread spectrum methods for mobile communication
4. Understand the working of global system for mobile (GSM), CDMA, WCDMA and blue tooth technology

Introduction to wireless digital communication systems; radio propagation and cellular engineering concepts; speech and video coding for wireless systems application.

Basic digital modulation methods; ASK, PSK and FSK; Quadrature multiplexing and its applications; advanced modulation methods.

Spread Spectrum methods: basics; generation and properties of PN sequences, DS-SS system analysis; slow and fast FH-SS system; performance analysis.

Carrier synchronization and tracking methods, Mth power loop, early-late gate method, advanced methods.

Diversity methods for Mobile Wireless Radio Systems:

concepts of diversity branch and signal paths, combining and switching methods, C/N and C/I ratio improvements, average Pe improvements

Cellular and wireless system engineering; Study of GSM, CDMA and W-CDMA networks; Study of Bluetooth technology.

Text Books:

1. Wireless Digital Communication: Feher K ;PHI
2. Digital communication (Third Edition): Proakis John ;Tata- McGraw-Hill.

Reference Books:

1. Digital communication: Haykin Simon;Wiley
2. Communication systems, Fourth Edition: Haykin Simon ;Wiley.

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code : ENT603-3 **Course : Advanced Embedded Systems**

L : 4 Hrs., P : 0 Hrs., Per week **Total Credits : 8**

Course Objectives :

The objective of this course is to provide students with

1. understanding of necessity of operating system in advanced embedded systems.
2. fundamental concepts of Real Time Operating Systems (RTOS) by identifying the challenges in real-time systems.
3. basic knowledge of various aspect of Linux as Embedded OS.

Course Outcome:

Upon the completion of this course, students will demonstrate the ability to:

I. interpret unique design problems as well as challenges of software architecture and real-time systems.
II. implement a RTOS based embedded system.
III. identify current issues in OS based embedded systems.

Syllabus

Introduction to Intellectual Property (IP) Cores, Core examples.

Concept and Fundamentals of RTOS, essential features, ROS Kernel Function, RTOS examples.

Interrupts, Handling an Interrupt, Interrupt Service Routines, Cooperative Multitasking, Context Switching, Process States, Multiple Threads, Communication Mechanism, Asynchronous Communication, Timesharing Operating Systems, Priority-based Scheduling, Typical RTOS Task Model, Rate-Monotonic Scheduling, EDF Scheduling, Priority Inversion, Priority Inheritance.

Inter-task Communication: Shared Variables, Monitors, Messages, Events, Semaphores, Priority inversion problem, Deadlocks, Starvation.

Linux as an embedded OS, Tools and development, Applications and products, The embedded OS market.

Text Books:

1. An embedded software primer: David E Simon, Pearson education Asia.
2. Micro C/OS II The Real Time Kernel: Jean J. Labrosse, CMP Books
3. Embedded System Design: Steve Heath, Butterworth Helnemann.

Reference Books:

1. Embedded System Design- A unified Hardware/software Introduction: Frank vahid/Tony Givargis,Wiley, 2002
2. Programming Embedded System in C and C++ : Michael Barr, O Reilly & Associates Inc.
3. The Art of Designing embedded system: Jack Ganssle, Newnes.

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code: ENP 604 **Course: Project Phase - I**

L: 0 Hrs., P : 6 Hrs., Per week **Total Credits : 24**

Course Objectives:

The objective of this course is to provide students with

1. Ability to perform need analysis of engineering Problems in industry and research.
2. Ability to apply techniques, skills, and modern EDA tools to identify, formulate and solve the engineering problems.
3. Ability to analyze research outcome and communicate it in effective manner with understanding of ethical, social and legal practices in profession.

Course Outcomes:

Upon completion of this course, students should demonstrate the ability to:

I. critically evaluate alternate assumptions, approaches, procedures, tradeoffs, and results related to engineering problems

II. apply engineering knowledge for design and implementation of VLSI based circuits and systems in an ethically responsible manner.

III. Use written and oral communications to document the research work and present results.

IV. Engage in self & life-long learning in continuing professional development.

SYLLABUS OF SEMESTER IV, M. Tech. (VLSI DESIGN)

Course Code: ENP 605 **Course: Dissertation / Thesis (Viva-Voce)**

L: 0 Hrs., P : 12 Hrs., Per week **Total Credits : 48**

Course Objectives:

The objective of this course is to provide students with

1. Ability to perform need analysis of engineering Problems in industry and research.
2. Ability to apply techniques, skills, and modern EDA tools to identify, formulate and solve the engineering problems.
3. Ability to analyze research outcome and communicate it in effective manner with understanding of ethical, social and legal practices in profession.

Course Outcomes:

Upon completion of this course, students should demonstrate the ability to:

I. critically evaluate alternate assumptions, approaches, procedures, tradeoffs, and results related to engineering problems

II. apply engineering knowledge for design and implementation of VLSI based circuits and systems in an ethically responsible manner.

III. Use written and oral communications to document the research work and present results.

IV. Engage in self & life-long learning in continuing professional development.