SHRI RAMDEOBABA COLLEGE OF ENGINEERING AND MANAGEMENT, NAGPUR - 440013

An Autonomous College affiliated to
Rashtrasant Tukadoji Maharaj Nagpur University,
Nagpur, Maharashtra (INDIA)

PROGRAMME SCHEME & SYLLABI
2017-19

M.TECH. (VLSI DESIGN)

Published by
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ISO 9001 : 2008 CERTIFIED ORGANISATION

About the Department:

Department of Electronics Engineering was established in 1986. The Department offers a UG programme in Electronics Engineering and PG programme in M.Tech. (VLSI Design). The National Board of Accreditation; New Delhi has accredited the UG programme thrice in succession in the year 2003, 2007 & 2013 and PG programme in 2016. It is recognized centre for Doctroal programmes of RTM Nagpur University and the department also admits candidates under Visvesvaraya Ph. D scheme. The students undergoes to projects in association with industries. The undergraduate students participate under RGSTC-TIFAC-MSME Internship Program. the department has received a grant of Rs. 10 lakhs from AICTE under its MODROB scheme to carry out projects in CMOS VLSI area. The Department has 16 state of the art labs with investment over Rs. 2 crore. The major sofware include VLSI design, development and verification platforms, such as Mentor Graphics Suite, SDSoC, COMSOL, Xilinx's ISE Development Platform, Tanner tool, ORCAD 15.7. The design Platforms include Virtex 5 Development platform and Embedded System Design environment like NIOS II, Embedded Evaluation CYCLONE III Platform, ARM 7/9/11, Cortex-M0/M4 Development Platforms. Advanced Communication trainers and test equipments include Fiber Optic Trainer, Spectrum Analyzer, Digital Storage Oscilloscope, MIC Trainer, Digital Signal Processors and simulation tools MATLAB 2013 R, Labview 8.0 are also part of the state - of - the art laboratories.

About the Programme :

M.Tech (VLSI Design) is a full time two year programme offered by Electronics Engineering Department wih an intake of 24 and started in year 2004. Programme is accredited by National Board of Accreditation, New Delhi. Programme is based on Choice Based Credit System (CBCS) where students can take courses of their choice, learn at their own pace, undergo additional courses, acquire more than the required credits and adopt an interdisciplinary approach to learning. The curriculum is well designed to expose the students to contemporary Digital, Analog, Embedded and RF system design using industry standard EDA tools and development platforms. Dedicated state - of - the - art laboratories include major software and hardware platforms for VLSI Design. Software tools such as Mentor Graphics backend and frontend suit, Tanner Tool, Keil MDK, COMSOL, SDSoC and hardware development platforms such as Xilinx, Altera, Freescale, Cypress, Texas are available.

In order to prepare post graduates to take gainful employment in core, allied sectors of Electronics Engineering, R & D organization and entrepreneurship, the curriculum components include hands-on training, core-elective courses and industry oriented projects.

Students undergo their internship at various R & D organizations, reputed academic institutions and industries such as Indian Nano-electronics Users Program (INUP) at IIT Bombay, IIT Gandhinagar, ISRO,BARC, Godrej, NEERI, IIIT Jabalpur, VNIT Nagpur etc.

Vision of Department

Electronics Engineering Department endeavors to facilitate state of the art technical education in the field of electronic engineering by infusing scientific by infusing scientific temper in students leading towards research and to grow as centre of excellence in the field of microelectronics.

Mission of Department

- To promote quality education through stimulating environment for dissemination of knowledge and technology.
- To impart necessary technical, professional skills with moral and ethical values to enable students for achieving a successful career.
- To develop centre of excellence in the field of microelectronics and its allied areas with continuing education program.
- To foster research and development in collaboration with institutions / industires.

Shri Ramdeobaba College of Engineering and Management, Nagpur-13

Department of Electronics Engineering

M. Tech. (VLSI Design)

(Choice Based Credit System)

Session 2017-2019

Program Objectives:

1. To develop graduates with an ability to design and analyze VLSI Systems.
2. To prepare graduates with necessary skills and knowledge of the discipline to excel in their career.
3. To encourage life-long learning with commitment to ethical practices.

Program Outcomes :

a) An ability to apply knowledge of mathematics, science, and engineering fundamentals appropriate to the discipline.

b) An ability to design and implement systems by critically analyzing and interpreting design specifications with socio-economic consideration.

c) An ability to function individually and in groups, including diverse and multidisciplinary fields, to accomplish a common goal.

d) An ability to identify, formulate and solve problems pertaining to discipline.

e) An understanding of professional and ethical responsibility.

f) An ability to communicate effectively.

g) An ability to engage in self, reflective, life-long learning in continuing professional development.

h) Knowledge of contemporary issues pertaining to discipline.

i) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practices.

j) An understanding of engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects.

k) An ability to apply appropriate research methodologies and contribute towards development of scientific knowledge in engineering discipline.

SCHEME OF EXAMINATION OF M. TECH (VLSI DESIGN)
SEMESTER PATTERN

I SEMESTER M. TECH (VLSI DESIGN)

Sr. No.	Code	Course	L	P	Credits	Maximum Marks			Exam Duration	Category
						Continuous Assessment	End Sem	Total		
1	ENT551	CMOS Digital Circuit Design	4	0	4	40	60	100	3 Hrs.	PC
2	ENT552	Digital System Design	4	0	4	40	60	100	3 Hrs.	PC
3	ENT553	Embedded System and RTOS	4	0	4	40	60	100	3 Hrs.	PC
4	ENT554	Semiconductor Devices	4	0	4	40	60	100	3 Hrs.	FC
5	ENP551	CMOS Digital Circuit Design Lab	0	2	1	25	25	50	----	PC
6	ENP552	Digital System Design Lab	0	2	1	25	25	50	----	PC
7	ENP553	Embedded System & RTOS Lab	0	2	1	25	25	50	----	PC
8	ENT555	Programme Elective-I	4	0	4	40	60	100	3 Hrs.	PE
		Total	**20**	**6**	**23**					

Course Code	Programme Elective - I
ENT555-1	VLSI Technology
ENT555-2	Advanced Computer Architecture
ENT555-3	Advanced Digital Signal Processing

II SEMESTER M. TECH (VLSI DESIGN)

Sr. No.	Code	Course	L	P	Credits	Maximum Marks			Exam Duration	Category
						Continuous Assessment	End Sem	Total		
1	ENT556	Analog IC Design	4	0	4	40	60	100	3 Hrs.	PC
2	ENT557	System Verilog for Verification	4	0	4	40	60	100	3 Hrs.	PC
3	ENT558	Research Methodology	3	0	3	40	60	100	3 Hrs.	FC
4	ENP556	Analog IC Design Lab	0	2	1	25	25	50	----	PC
5	ENP557	System Verilog for Verification Lab	0	2	1	25	25	50	----	PC
6	ENT559	Programme Elective-II	4	0	4	40	60	100	3 Hrs.	PE
7	ENT560	Group Elective-I	4	0	4	40	60	100	3 Hrs.	GE
8	ENT599	Open Elective-I	3	0	3	40	60	100	3 Hrs.	OE
9	ENP561	Seminar	0	2	1	50		50	----	PC
		Total	**22**	**6**	**25**					

Course Code	Programme Elective - II
ENT559-1	VLSI Signal Processing
ENT559-2	RF Circuit Design
ENT559-3	MEMS

Course Code	Group Elective-I
ENT560	VLSI Design Automation
EET561	Electrical Power Distribution & Smart Grid
CST561-1	Optimization Techniques in Artificial Intelligence
CST561-2	Social Network Analysis

Course Code	Open Elective-I
ENT599-2	Digital System Design with FPGA

III SEMESTER

Sr. No.	Code	Course	L	P	Credits	Maximum Marks			Exam Duration	Category
						Continuous Assessment	End Sem	Total		
1	ENT651	System-on-Chip	4	0	4	40	60	100	3 Hrs.	PC
2	ENT652	Programme Elective-III	4	0	4	40	60	100	3 Hrs.	PE
3	ENP653	Project Phase I	0	3	6	50	50	100	----	PC
		Total	**8**	**3**	**14**					

Course Code	Programme Elective-III
ENT652-1	VLSI Testing
ENT652-2	Nanoelectronics
ENT652-3	Low Power VLSI Design

IV SEMESTER

Sr. No.	Code	Course	L	P	Credits	Maximum Marks			Exam Duration	Category
						Continuous Assessment	End Sem	Total		
1	ENP654	Project Phase-II	0	6	12	150	150	300	----	PC
		Total	**0**	**6**	**12**					

SYLLABUS OF SEMESTER I, M. TECH. (VLSI DESIGN)

Course Code : ENT551 — **Course : CMOS Digital Circuit Design**

L : 4 Hrs., P : 0 Hrs., Per week — **Credits : 4**

Course Objectives:

The objective of this course is to provide students with

1. Knowledge of circuit models for analysis of digital CMOS circuits and interconnect.
2. Implementation technique necessary to realize CMOS circuits/ Sub-systems using various CMOS logic structures.
3. Computation methods required for circuit characterization and performance estimation.
4. Understanding of various CMOS processes and emerging nanometer-scale technologies.

Course Outcomes:

Upon completion of this course, students should demonstrate the ability to:

I. Apply the circuit models to investigate CMOS circuits.
II. Design moderately sized CMOS circuits/ sub-systems and compute timing, power and parasitics for various CMOS Logic structures.
III. Evaluate various micron, deep sub-micron and nanometer-scale technologies.

Syllabus:

Introduction to MOS Transistors, Switches, CMOS Logic, Scaling and transistor structures for VLSI; Silicon-on-insulator transistors.

Static Load MOS Inverters, CMOS Inverter, Tri State Inverter.

Circuit Characterization and Performance Estimation: Introduction, Resistance Estimation, Capacitance Estimation, Switching Characteristics, Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing.

CMOS Circuit and Logic Design: CMOS Logic Gate Design, CMOS Logic Structures, Clocking Strategies, I/O Structures, Driving Large capacitive loads.

CMOS Sub System Design: Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Binary Counters, ALUs, Multiplication, Shifters, Memory Elements, Control-FSM, Control Logic Implementation.

Memory elements: Read write memory, RAM, Register files, FIFO, LIFO, SIPO, Serial access Memory, CAM, ROM.

Text books:

1. Principles of CMOS VLSI Design: *N. Weste and K. Eshranghian, , Addison Wesley, 2nd Edition*
2. Digital Integrated Circuits: *A Design Perspective: J. Rabaey, PHI, 2nd Edition*
3. Basic VLSI Systems and Circuits*: Dougles Pucknell and K. Eshraghian PHI, 3rd Edition*

Reference books:

1. VLSI Analog and Digital Circuit Design Techniques: *Randel & Geiger TMH*
2. Introduction to VLSI System: *Carver Mead, Lynn Conway, Addison-Wesley, 1st Edition*
3. CMOS Digital Integrated Circuits Analysis & Design: *S M Kang, Yusuf Leblebici, TMH, 3rd Edition (2003)*

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENP551 **Course : CMOS Digital Circuit Design Lab**
L : 0 Hrs., P : 2 Hrs., Per week **Credits : 1**

Practicals / Case Studies / Mini projects based on syllabus of ENT551

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: ENT552 **Course: Digital System Design**
L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Objective

The objective of this course is to provide students with

1. Concept of modeling and testing the digital designs using HDL
2. Idea of digital system design flow
3. Synthesis and optimization techniques for digital designs
4. Knowledge of timing analysis and programmable devices

Course Outcome

Upon the completion of this course, students will demonstrate the ability to:

I. Model and test the digital designs
II. Describe the digital system design flow
III. Write a optimize and synthesizable HDL code
IV. Analyze the timing issues and implement the digital logic on various programmable devices

Syllabus:

Hardware Description Languages: Introduction to HDL, Basic Language Elements, Syntax and Semantics HDL, Modeling Styles for building blocks, use of Procedures –functions / Task –function in designs, Attributes, Writing Test Benches, Handling Text files, Combinational & Sequential Design examples : Adders, Multipliers, ALU, Memories, FSM, FIFO

System Design Flow: Top-Down and Bottom-Up methodology, Word Length Determination, Data Path Control Path, Implementation of DSP algorithm

Synthesis - Analysis and Introduction to Optimization Techniques: Methodology, Logic Synthesis of HDL, Critical Path analysis, Speed, Area and Power optimizations at Architectural level

Timing and Signal Integrity: Timing Basics and Signal integrity, Dealing with Clock Skew and Jitter, Synchronizers

Programmable ASICs: Technology Overview, CLBs, Architecture, Realization of functions

Text books:

1. A VHDL Primer, Third Edition: J. Bhasker, *Prentice Hall, (1999).*
2. Verilog HDL: A guide to Digital Design and Synthesis: Samir Palnitkar*, Prentice Hall(1996)*
3. Advanced Digital Design with the Verilog HDL: M.D. Ciletti*, Prentice Hall, (2003).*
4. Synthesis and Optimization of Digital Circuits, G. De Micheli, *McGraw-Hill, (1994).*

Reference books:

1. The Verilog Hardware Description Language, Fifth Edition: Donald E. Thomas, Philip R. Moorby, *Kluwer Academy Publisher. (2002).*
2. Digital Systems Design Using VHDL, Second Edition: Charles H. Roth. Jr., L Kurian John, *Cengage Learning, (2008).*
3. Logic Synthesis using Synopsys, Second edition, P. Kurup and T. Abbasi, *Kluwer, (1996)*
4. Logic synthesis and verification algorithms: Gary D. Hachtel, Fabio Somenzi, *Springer (1996)*
5. An Engineering Approach to Digital Design: *W. Fletcher. Prentice Hall*

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENP552 **Course : Digital System Design Lab.**
L : 0 Hrs., P : 2 Hrs., Per week **Credits : 1**

Practicals / Case Studies / Mini projects based on syllabus of ENT552

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: ENT553 **Course: Embedded System and RTOS**
L :4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Objectives:
The objective of this course is to provide students with

1. Understanding of ARM architecture and its organization.
2. Interfacing and Programming concepts of ARM based microcontroller.
3. Fundamental concepts of Real Time Operating Systems (RTOS)
4. Knowledge of various aspects of COS and Linux as Embedded OS.

Course Outcomes:
Upon the completion of this course, students will demonstrate the ability to:

I. Apply the knowledge of ARM architecture and organization for modern ARM Contex - M devices.
II. Utilize knowledge, techniques & skill to integrate microcontroller hardware and software component using Contex - Mo.
III. Apply the concepts of Embedded OS.
IV. Implement OS based embedded system.

Syllabus:
Introduction to Embedded Systems, Concepts, Embedded System Design Issues. RISC Principles.
The Cortex - M processor: Applications, Simplified view – block diagram, programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence, Instruction Set, Unified Assembler Language, Pipeline, Bus, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, SYSTICK Timer, Interrupt Sequences, Introduction to the Cortex microcontroller software interface standard (CMSIS), Interfacing of GPIOs, Timers, ADC, UART and other serial interfaces, PWM.
Concept and Fundamentals of RTOS: RTOS examples, Interrupts, Handling an Interrupt, Interrupt Service Routines, Context Switching, Process States, Communication Mechanism, Scheduling Algorithm, Priority Inversion, Priority Inheritance. Inter-task Communication: Shared Variables, Monitors, Messages, Events, Semaphores, Priority inversion problem, Deadlocks, Starvation.
Concepts, Structure of COS - II: - Kernel Structure: Tasks, Task States, TCB, Ready List, Task Scheduling, Interrupts, Clock Tick, Initialization, Starting the OS, Task Management, Time Management, Event Control Blocks, Synchronization in COS - II: - Semaphore Management, Mutual Exclusion Semaphores, Event Flag Management, Communication in COS - II: - Message Mailbox Management, Message Queue Management, Memory management, Porting of COS – II
Linux as an embedded OS, Tools and development, Applications and products, Building Linux Kernel

Text Books:

1. The Definitive Guide to the ARM Cortex-M0 : Joseph Yiu, Elsevier , (1/E)2011
2. An Embedded Software Primer: David E Simon, Pearson education Asia, 2001
3. Micro C/OS II The Real Time Kernel: Jean J. Labrosse, CMPBooks,(2/E) 2002
4. Embedded Linux Primer: christopher Hallinan, Pearson (1/E) 2007

Reference Books:

1. ARM System Developer's Guide Designing and Optimizing System Software: Andrew N. Sloss, Dominic Symes, Chris Wright, Morgan Kaufmann publications, (1/E) 2004.
2. ARM system on chip Architecture: Steve Furber, Pearson Education Addison Wesley, (2/E) 2000

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENP553 **Course : Embedded System and RTOS Lab**

L : 0 Hrs., P : 2 Hrs., Per week **Credits : 1**

Practicals/ Case Studies/ Mini projects based on syllabus of ENT553

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENT554 **Course : Semiconductor Devices**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Objectives:

The objective of this course is to provide students with

1. Essentials of semiconductor physics to mathematically analyze PN junctions, and MOSFETs.
2. Understanding of various semiconductor device models and parameters.
3. Insight useful for understanding new semiconductor devices and technologies.

Course Outcomes:

Upon completion of this course, students should demonstrate the ability to

I. Utilize semiconductor models to analyze carrier densities and carrier transport.
II. Understand and utilize the basic governing equations to analyze semiconductor devices.
III. Understand and analyze the inner working of semiconductor p-n diodes, Schottky barrier diodes and advanced MOSFET technology.

Syllabus:

Basic Semiconductor Physics

Crystal lattice, energy band model, density of states, distribution statics – Maxwell-Boltzmann and Fermi-Dirac, doping, carrier transport mechanisms, drift, diffusion, thermionic emission, and tunneling; excess carriers, carrier lifetime, recombination mechanisms – SHR, Auger.

p-n junction and metal-semiconductor junction

p-n junctions - fabrication, basic operation – forward and reverse bias, DC model, charge control model, I-V characteristics, steady-state and transient conditions, capacitance model, reverse-bias breakdown, SPICE model; metal-semiconductor junctions –fabrication, Schottky barriers, rectifying and non-retifying contacts, I-V characteristics.

MOS Capacitors and MOSFETs

The MOS capacitor – fabrication, surface charge – accumulation, depletion, inversion, threshold voltage, C-V characteristics – low and high frequency; the MOSFET – fabrication, operation, gradual channel approximation, simple charge control model (SCCM), Pao-Sah and Schichman – Hodges models, I-V characteristics, second-order effects – Velocity saturation, short-channel effects, charge sharing model, hot-carrier effects, gate tunneling; subthreshold operation – drain induced barrier lowering (DIBL) effect, unified charge control model (UCCM), SPICE level 1, 2, and 3, and Berkeley short-channel IGFT model (BSIM).

Advanced MOSFET technology: SOI MOSFET, high-k MOS devices, FinFETs and Multi gate MOSFETs

Text Books:

1. Physics of Semiconductor Devices: *S. M. Sze, Wiley Eastern, (1981).*
2. Semiconductor physics and Devices, Donald Neamen, McGraw-Hill, 3rd edition
3. Solid State Electronic Devices ,B.G.Streetman and S.Banerjee ,Prentice Hall India

Reference Books:

1. CMOS Circuit Design, Layout and simulation: *J. Baker, D.E. Boyce., IEEE press*.

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENT555-1 **Course : VLSI Technology**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Objectives:

The objective of this course is to provide students with

1. Knowledge of the scientific principles involved in fabrication of integrated circuits.
2. Understanding of fabrication steps involved in fabrication process of MOSFET.
3. A comprehensive understanding of process integration and manufacturing for integrated circuits.

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

I. Plan a sequence of processing steps to fabricate a solid state device to meet geometric, electrical, and/or processing parameters.
II. Design VLSI circuits by keeping technological process constraints in mind.
III. Understand the relevance of a process or device, either proposed, past or existing, to current manufacturing practices.

Syllabus:

Environment for VLSI Technology: Clean room and safety requirements, Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation: Solid State diffusion modeling and technology; Ion Implantation modeling, technology and damage annealing; characterization of impurity profiles.

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films, Oxidation technologies in VLSI and ULSI; Characterization of oxide films, High k and low k dielectrics for ULSI.

Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

Chemical Vapor Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modeling and technology.

Metal film deposition: Evaporation and sputtering techniques, Failure mechanisms in metal interconnects; Multi-level metallization schemes.

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.

Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technologies.

Text Books

1. ULSI Technology: *C. Y. Chang and S. M. Sze (Ed), McGraw Hill Companies Inc, (1996).*
2. VLSI Fabrication Principles: *S. K. Ghandhi, John Wiley Inc., New York, (1983).*
3. VLSI Technology 2nd ed.: *S. M. Sze (Ed), McGraw Hill, (1988).*

Reference Books:

1. Physics of Semiconductor Devices: *S. M. Sze, Wiley Eastern, (1981).*

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENT555-2 **Course : Advanced Computer Architecture**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Objectives:

The objective of this course is to provide students with:

1. Comprehensive understanding of scalable and parallel computer architectures for achieving a proportional increase in performance with increasing system resources.
2. Understanding of superscalar, vector processors and super pipelining technologies.
3. Broad understanding of the concept of Multiprocessor and multicomputer architectures.
4. Knowledge of advanced processor technology, memory hierarchy and design of pipelined processors.

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to

I. Define the principles of computer design and its performance enhancement measures.
II. Describe the performance improvement techniques such as pipelining, dynamic scheduling, branch predictions, and cache.
III. Describe the modern architecture such as RISC, Scalar, VLIW, Multi core and multi CPU systems.
IV. Appraise memory organizations and modern computer architectures.

Syllabus:

- Classes of computers, Trends in technology, power and costs, dependability, quantitative principles of computer design, Models of parallel computer, multiprocessors and multi-computers, multi-vector and SIMP computers, PRAM and VLSI model, conditions of parallelism, data and resource dependencies, grain size and latency, grain packing and scheduling, program flow mechanisms, system interconnect architectures.
- Principles of scalable performance, performance metrics and measures, speedup performance laws, advanced processor technology, superscalar and vector processors, cache memory organizations, shared memory organizations.
- Pipeline and superscalar techniques, linear pipeline processors, reservation and latency analysis, collision free scheduling, pipeline schedule optimization, instruction pipeline design, arithmetic pipeline design, superscalar and super-pipeline design.
- Multiprocessors and multi computers, multiprocessor system interconnects, cache coherence and synchronization mechanisms, message passing schemes.
- Multi-vector and SIMD computers vector processing principles, compound vector processing, SIMD computer organizations scalable multithreaded and dataflow architectures.
- Elementary theory about dependence analysis, techniques for extraction of parallelism.

Text Books :

1. Advanced Computer Architecture: *Kai Hwang; McGraw Hill.*
2. Computer Architecture: A Quantitative Approach: J. Hennessy and D. Patterson, Morgan Kaufmann, 3rd edition, 2003.
3. Advanced Computer Architecture and Computing: *S.S. Jadhav, Technical Publication, Pune*

Reference Books:

1. Advanced Computer Architectures: A Design Space Approach: Dezso Sima, Terence Fountain, Peter Karsuk, Pearson Education, 1st edition, 1997.
2. Advanced Computer Architecture: *Richard Y. Kausi ; Prentice Hall of India*

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : ENT555-3 **Course : Advanced Digital Signal Processing**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Objectives:

The objective of this course is to provide students with

1. Knowledge of multirate signal processing
2. Understanding of programmable DSP processor
3. Awareness of algorithmic strength reduction techniques
4. Knowledge of applications in DSP

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

I. Analyze the multirate digital signal processing architectures
II. Describe the architecture of programmable DSP processor
III. Reduce the computational complexity of the signal processing algorithms
IV. Illustrate the applications of DSP

Syllabus:

Basics of Signal Processing and Multirate Signal Processing

Basics of signal Processing, Multirate Signal Processing: analysis of multirate structures, multistage design of decimator and interpolator, computationally efficient interpolator and decimator structures, Design of linear phase/poly-phase FIR filters.

Programmable DSP (P-DSP) Processor : Evolution of (P-DSP) processors and features, multiport memory , Architectural structural of (P-DSP) :MAC units, Barrel Shifters, Introduction to DSP processor family for multimedia signal processing ,SIMD, MIMD, VLIW architecture.

Algorithmic strength Reduction in Filters :

Parallel FIR filters: formulation using polyphase decomposition, Fast FIR algorithms

Algorithm -Architecture Transformation : DCT -IDCT

Parallel Architecture for Rank order filters

Applications of DSP:

Dual Tone Multifrequency Signal Detection, Spectral Analysis of Sinusoidal signal and non stationary signals

Sound Processing : echo filtering, reverberator architecture, flanging, chorus generator Oversampling A/D and D/A convertor.

Text Books

1. Digital Signal Processing : Principles, Algorithms and Applications PHI publications 4th Edition, John G. Proakis, Dimitris G. Manolakis.
2. VLSI Digital Signal Processing Systems: Design and Implementation Wiley India Edition, By K.K. Parhi.
3. Digital Signal Processing : A computer Based Approach, Mcgraw Hill 3rd Edition, By Sanjit K. Mitra.

Reference Books:

1. Discrete Time Signal Processing, Pearson Prentice Hall India, 2nd edition, A.V. Oppenheim, R. W. Schaefer.

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENT556 **Course : Analog IC Design**
L: 4 Hrs, P: 0 Hrs. Per week **Credits: 4**

Course Objectives:

The objective of this course is to provide students with

1. Sound understanding of complementary metal-oxide-semiconductor field-effect transistor and the relationship of process technology with models used for analog IC.
2. Analysis, up to and including second - order effects caused by scaling of CMOS technology and modeling deficiencies.
3. Techniques for analyzing and designing a variety of analog circuits in CMOS technology.

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

I. Use mathematical models of MOS transistors to evaluate their behavior in analog circuits.
2. Select suitable design approaches while trading off conflicating requirements.
3. Investigate various analog IC performance parameters.

Syllabus:

Introduction to analog VLSI and analog design issues in CMOS technologies.

Basic analog building blocks : Switches, Active resistors, current, voltage sources and sinks, current mirrors, current and voltage reference, Bandgap references.

Amplifiers, Common source, source flower, common gate and cascode amplifiers, Frequency Response.

Frequency Response of Amplifiers : Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers.

Differential Amplifier - Basic Differential Pair, common mode response, CMRR, Differential Pair with MOS load, Gilbert Cell.

OPAMP Design : Single stage and two Stage OP-Amps, Frequency Compensation.

Switch Capacitor circuits : General Considerations, sampling switches, Switched capacitor integrator.

Text Books:

1. Design of Analog CMOS IC : B Razavi, Tata Mcgraw Hill (2002)
2. CMOS Circuit Design, Layout and Simulation : J. Baker, D.E. Boyee., IEEE press (2010).
3. VLSI Design techiques for Analog and digital Circuits : R. L. Geiger, P.E. Allen, D.R. Holberg, OUP (2/E) McGraw Hill (2002)

Reference Books :

1. VLSI Design techniques for Analog and digital Circuits : Randel Geiger, P. Allen, N. Strader, Tata Mcgraw, Hill, (2/E) (2010)
2. Analysis and Design of Analog ICs : Paul R. Gray, Paul J. Hurst Stephen H. Lewis, Robert G. Meyer, J, Willy and Sons, (4/E) (2001)

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENP556 **Course : Analog IC DesignLab.**
L : 0 Hrs., P : 2 Hrs., Per week **Credits : 1**

Practicals/ Case Studies/ Mini projects based on syllabus of ENT556

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: ENT557 **Course: System Verilog for Verification**

L : 4 Hrs., P : 0 Hrs., Per week **Total Credits : 4**

Course Objectives:

The objective of this course is to provide students with

1. Insight to apply System Verilog concepts to do synthesis, analysis and architecture design.
2. Understanding of SystemVerilog and SVA for verification, and understand the improvements in verification efficiency.
3. Understand advanced verification features, such as the practical use of classes, randomization, checking, and coverage.
4. Knowledge to communicate the purpose and results of a design experiment in written and oral presentations.

Course Outcomes:

Upon completion of this course, students should demonstrate the ability to

I. Use SystemVerilog to create correct, efficient, and re-usable models for digital designs

II. Use SystemVerilog to create testbenches for digital designs

III. Understand and effectively exploit new constructs in SystemVerilog for verification

Syllabus:

Verification Guidelines: Introduction, Verification Process, Verification Plan, Verification Methodology Manual, Basic Testbench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Testbench Components, Layered Testbench,

Data Types: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Creating New Types with typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings

Procedural Statements And Routines: Procedural Statements, Tasks, Functions, and Void Functions

Basic Object Oriented Programming: Where to Define a Class, OOP Terminology, Understanding Dynamic Objects

SystemVerilog Assertions: Types of Assertions and examples

Threads and Inter-process Communication: Working with Threads, Inter-process Communication, Events, Semaphores, Mailboxes, Building a Testbench with Threads and IPC

Functional Coverage: Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Coverage Options, Parameterized Cover Groups, Analyzing Coverage Data, Measuring Coverage Statistics During Simulation

Introduction to formal verification: Introduction to formal techniques and property specification, Reachability analysis, Elements of property languages, Property language layers, PSL basics, Formal test plan process, Techniques for proving properties: Abstraction reduction, Compositional reasoning, Counter abstraction, Gradual Exhaustive formal verification.

Text books :

1. System Verilog for Verification: A Guide to Learning the Testbench Language Features, Chris Spear, Springer 2006
2. Writing Testbenches Using SystemVerilog, Janick Bergeron, Springer, 2006
3. SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, 2nd Edition, Stuart Sutherland, Simon Davidman and Peter Flake, Springer

Reference books:

1. Writing Testbenches: Functional Verification of HDL Models, Second edition, Janick Bergeron, Kluwer Academic Publishers, 2003.
2. Open Verification Methodology Cookbook, Mark Glasser, Springer, 2009
3. Principles of Functional Verification, Andreas S. Meyer, Elsevier Science, 2004
4. Assertion-Based Design, 2nd Edition, Harry D. Foster, Adam C. Krolnik, David J. Lacey, Kluwer Academic Publishers, 2004.

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENP557 **Course : System Verilog for Verification Lab**
L : 0 Hrs., P : 2 Hrs., Per week **Credits : 1**

Practicals / Case Studies / Mini projects based on syllabus of ENT557

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENT558 **Course : Research Methodology**
L : 3 Hrs., P : 0 Hrs., Per week **Credits : 3**

Course Objectives:

The objective of this course is to provide students with:

1. An insight into how scientific research is conducted
2. Knowledge of Research Process, Concepts, diverse research tasks and equip them to undertake research.
3. Understanding the concepts of Data collection, system modeling and reliability.
4. To develop an understanding for the optimization methods in research work.
5. Methods for presentation of research results.

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

I. Evaluate current research and propose possible alternate directions for further work.
II. Develop hypothesis and methodology for research
III. Enhance the performance of research by optimization methods.
IV. Comprehend and deal with complex research issues in order to communicate their scientific results clearly for peer review.

Syllabus:

Research: Research Process, Research Concept and demonstration of different types of research task

Research design and hypothesis: Problem identification and formulation, hypothesis types and verification, methods of research.

Data collection and Modeling: Literature review, data analysis, Logic / Experimental / Field data based modeling, modeling based on design of new system / Process / Product, Modeling based on Statistical Concepts.

System modeling: Simulation modeling, verification & validation of model, Validation of results, optimization of model and case studies.

Reliability of Established Model: Review of theory of reliability, Hazard models, System Reliability.

Optimization Techniques: Introduction of Taguchi method, Steps involved in Taguchi method and its applications for process parameters, Analysis of Variance (ANOVA), its significance and applications.

Report writing and outcome: Structure and contents of report, presentation of findings, formats of report writing, formats of publication in research journals, Referencing in academic writing, Ethics in research, electronic and internet sources, Intellectual Property.

Text Books

1. Angela Dean & Daniel Voss, Design & Analysis of Experiments, Published by Springer-Verlag New York, In
2. H. Schenck Jr., Theories of Engineering Experimentation, Mc-Graw Hill, First Edition
3. Law, A. M. and W. D. Kelton, 1991, Simulation Modeling and Analysis, Second Edition, McGraw-Hill
4. Kothari C.K. (2004), 2/e, Research Methodology Methods & Techniques (New Age International, New Delhi).

Reference Books

1. Banks, J. J., S. Carson and B. L. Nelson. 1996. Discrete event system simulation. 2d ed. Upper saddle river, New Jersey: Prentice-Hall.
2. Montgomery, Douglas C. (2007), 5/e, Design and Analysis of Experiments, (Wiley India)
3. Montgomery, Douglas C. & Runger, George C. (2007), 3/e, Applied Statistics & Probability for Engineers (Wiley India).

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENT559-1 **Course : VLSI Signal Processing**

L : 4 Hrs., P : 0 Hrs., Per week **Credits: 4**

Course Objectives:

The objective of this course is to provide students with

1. Concepts of pipelining, parallel processing, retiming, folding and unfolding for digital signal processing architectures.
2. Knowledge of systolic architecture
3. Analysis to optimize fast convolution algorithms for digital signal processing architectures in terms of computational complexity.

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

I. Apply the concepts of pipelining, parallel processing, retiming, folding and unfolding to optimize digital signal processing architectures.
II. Analyze data flow in systolic architectures.
III. Minimize the computational complexity using fast convolution algorithms.

Syllabus:

Introduction to Digital Signal Processing Systems: Introduction, Typical DSP Algorithms, Representations of DSP Algorithms.

Iteration Bound: Introduction, Data Flow Graph Representations, Loop Bound and Iteration Bound, Algorithms for Computing Iteration Bound, Iteration Bound of Multirate Data Flow Graphs.

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing. Pipelining and Parallel Processing for Low Power.

Retiming: Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques.

Unfolding: Introduction, Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming, Applications of Unfolding.

Folding: Introduction, Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR systolic Arrays, Selection of scheduling vector, Matrix-Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations containing Delays.

Fast Convolution: Introduction, Cook-Toom Algorithm, Winogard Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

Text Books :

1. VLSI Digital Signal Processing Systems: Design and Implementation *Keshab K. Parhi. John Wiley-Inter science. publication (1999).*
2. Analog VLSI Signal & information processing: *Mohammed Ismail, Terri, Fiez, McGraw Hill. (1994).*

Reference Books:

1. VLSI and Modern Signal Processing: *kung. S. Y., H. J. White house T. Kailath, prentice hall, (1985).*
2. Design of Analog Digital VLSI circuits for telecommunications and signal processing: *Jose E. France, Yannis Tsividls, prentice Hall, (1994).*

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: ENT559-2 **Course : RF Circuit Design**
L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Objectives:

The objective of this course is to

1. Provide understanding of modern RF electronics devices, employed in RF Receiver Design
2. Make familiar with issues encountered in high-frequency circuits, such as impedance matching, realization of passive components.
3. Provide understanding of architecture, specifications of RF transceiver and performance/testing issues like gain, isolation, Noise Figure, Linearity measures IIP3, 1dB compression, and SFDR.
4. Provide understanding of different topologies, major design issues and approaches of receiver blocks like noise amplifiers, mixers, power amplifiers and oscillators.
5. Use EDA tool and techniques for RF design.

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

I. Understand the architectures, operation and performance specifications/ tradeoff of a RF receiver and its building blocks.
II. Design and analyze impedance transformation networks using passive elements with smith charts and hand calculation.
III. Understand and evaluate various performance specifications for individual blocks of receiver like filters, LNA, Mixer, Power Amplifiers by hand calculations.
IV. Understand the sources of nonlinearity, noise, process technology and its impact on the performance parameters of individual blocks of receiver and on receiver performance.
V. Demonstrate the tools and techniques to evaluate the performance specifications of RF building blocks.

Syllabus:

Characteristics of passive components for RF circuits. Passive RLC networks. Transmission lines. Two-port network modeling. S-parameter model. The Smith Chart and its applications.

Active devices for RF circuits: SiGe MOSFET, GaAs pHEMT, HBT and MESFET. PIN diode. Device parameters and their impact on circuit performance.

Review of analog filter design: Low-pass, high-pass, band-pass and band-reject filters.

RF Amplifier design, single and multi-stage amplifiers.

Low Noise Amplifier design: noise types and their characterization, LNA topologies, power match vs noise match. Linearity and large-signal performance.

RF Power amplifiers: General properties. Class A, B, AB, C, D, E and F amplifiers. Modulation of power amplifiers.

Analog communication circuits: Mixers, phase-locked loops, oscillators, Transreceiver Architecture and performance specification.

Text Books:

1. The Design of CMOS Radio Frequency Integrated Circuits: *Thomas H. Lee- Cambridge University Press.*

Reference Books:

1. RF Microelectronics: Behzad Razavi- *McGraw Hill.*
2. Design of Analog CMOS integrated circuits*: Behzad Razavi- McGraw Hill.*
3. RF Circuit Design: Theory & Applications*: Reinhold Ludwig, Gene Bogdanov, Pearson India.*

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENT559-3 **Course : MEMS**
L : 4 Hrs., P : 0 Hrs., Per week **Total Credits : 4**

Course Objectives:

The objective of this course is to provide students with

1. Fundamental understanding of standard microfabrication techniques
2. Understanding of working principles of microsensors, actuators used in microsystems.
3. Major classes, components, and applications of MEMS devices/systems

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to

I. Apply the principles behind the operation of MEMS devices
II. Choose a micromachining technique for a specific MEMS fabrication process
III. Design and fabricate MEMS devices or a microsystem
IV. Understand recent advancements in the field of MEMS and devices.

Syllabus:

Micro-fabrication and Micromachining: Integrated Circuit Processes, Bulk Micromachining: Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA)

Physical Micro-sensors: Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors

Micro-actuators : Electromagnetic and Thermal micro-actuation, Mechanical design of micro-actuators, Micro-actuator examples, micro-valves, micro-pumps, micro-motors-Micro-actuator systems : Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector

Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micromachined Systems: Success Stories, Micromotors, Gear trains, Mechanisms

Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays.

MEMS for RF Applications: Need for RF MEMS components in communications, space & defense applications.

Text Books

1. Micro and Smart Systems, Ananthasuresh, G. K., Vinoy, K. J. Gopala Krishnan, S., Bhat, K. N., Aatre, V. K., Wiley-India, New Delhi, 2010. 1st Edition
2. RF MEMS and Their Applications: Vijay. Varadan, K. J. Vinoy, K. A. Jose, Wiley, 2002, 1st Edition.

Reference Books

1. Microsensors, MEMS and Smart Devices, Julian W. Gardner, Vinay K. Varadan, Osama O. Awadelkarim, Wiley, 2001, 1st Edition
2. VLSI Technology, Sze S. M., Mc Graw Hill, 2nd Edition

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: ENT560 **Course: VLSI Design Automation**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Objectives:

The objective of this course is to provide students with:

1. Fundamental Knowledge of VLSI CAD tool chain.
2. Techniques of Partitioning, floor-planning and routing
3. Basic Concepts of High level Synthesis

Course Outcomes:

Upon completion of this course, students should demonstrate the ability to:

I. Describe the VLSI design flow
II. Explain the algorithms for partitioning, floorplaning, placement and routing the digital designs.
III. Compare the various scheduling algorithms

Syllabus:

Introduction to VLSI CAD: VLSI design methodologies, use of VLSI CAD tools, Algorithmic Graph Theory and computational Complexity.

Partitioning: Introduction, Types of Partitioning, Classification of partitioning Algorithm, KL algorithm, FM algorithm etc.

Floorplanning: Introduction, Sliced and non-sliced planning, Polish expression

Placement: Introduction, Classification of Placement Algorithms: Simulated annealing, partition based placement

Routing: Fundamental Concepts such as Maze running, Line Searching, Steiner trees, Two phases of Routing: Global routing & detailed routing, Routing Algorithms

High-level Synthesis: Hardware Models for High-level Synthesis, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, ASAP, Mobility based Scheduling, List scheduling, Force directed scheduling

Basic Concepts of Static Timing Analysis

Text Books:

1. Algorithms for VLSI Design Automation:Sabih H. Gerez and John Wiley,(1998).
2. An Introduction to VLSI Physical Design: Majid Sarrafzadeh and C. K. Wong, McGraw Hill, (1996).
3. Algorithms for VLSI Physical Design Automation: NaveedSherwani, Kluwer Academic Pub., (1999).

Reference Books:

1. Physical Design Essentials: An ASIC Design Implementation Perspective: KhosrowGolshan, Springer, (2007)
2. Handbook of Algorithms for Physical Design Automation: Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, CRC Press, (2008).
3. Static Timing Analysis for Nanometer Designs: A Practical Approach: J. Bhasker and Rakesh Chadha, Springer, (2009).
4. Advanced ASIC Chip Synthesis: Using Synopsys Design Compiler, 2nd Edition: HimanshuBhatnagar, Kluwer Academic, (2001).

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

ELECTRICAL POWER DISTRIBUTION & SMART GRID

Course Code: EET561 **Course: Electrical Power Distribution & Smart Grid**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Pre-requisites:

Before studying this course, student should know the following concepts.

1. Basics of electrical engineering & technical problems of power systems.
2. Basics of power generation, distribution and grid.
3. Methods/tools used for different measurements and controls.
4. Electrical switch gears and their functions.

Course Objectives:

1. Students will understand the various aspects of distribution system, energy forecasting and load forecasting techniques
2. Students will understand automation in electrical power distribution
3. Students will understand the working of sectionalizing switch and network reconfiguration.
4. Students will understand the use of SCADA in distribution system.
5. Students will understand the working of Smart Grid.

Course Outcomes:

After the completion of this course, student will be able to,

CO1. Forecast the load & energy taking into consideration the available resources and smart techniques.
CO2. Identify the problems related with automation and SCADA and suggest suitable solution.
CO3. Understand the problems of restoration/ reconfiguration.
CO4. Describe real time schedule of operation of sectionalizing switches.
CO5. Distinguish between conventional grid and different types of smart grid
CO6. Discuss the use of smart technologies in smart grid.

Syllabus:

Load and Energy Forecasting: Distribution of power, Management, Power loads, Load forecasting, Power system loading, Technological forecasting. Need Based Energy Management (NBEM) – Objectives, Advantages, Distribution Management System (D.M.S.)

Distribution Automation: Definition, Restoration / Reconfiguration of distribution network Different methods and constraints. Interconnection of Distribution, Control & Communication Systems.

SCADA: Introduction, Block diagram, SCADA applied to distribution automation. Common Functions of SCADA, Advantages of Distribution Automation through SCADA.

Calculation of optimum number of switches, capacitors, Optimum Switching Device Placement in Radial. Distribution Systems. Sectionalizing Switches – Types, Benefits. Bellman's Optimality Principle, Remote Terminal Units.

Smart Grid: Introduction to Smart Grid, Definitions, Need, Functions, Opportunities & Barriers of Smart Grid, Difference between conventional & smart grid, Concept of Resilient & Self - Healing Grid, Present development & International policies in Smart Grid. Smart Grid Technologies: Smart Meters, Real Time Pricing, Smart Appliances, Automatic Meter Reading (AMR), Outage Management System (OMS), Smart Sensors, Smart Substations, Smart storage like Battery, SMES, Micro grids and Distributed Energy Resources.

Text books :

1. Electric Power Distribution: 4th ed.: *Pabla A.S., Tata McGraw Hill., New Delhi (2000).*
2. Learning Material for Electrical Power Distribution: *Khedkar M.K., (2004)*.
3. Smart Grid: Technology and Applications, Janaka Ekanayake, Nick Jenkins, Kithsiri Liyanage, Jianzhong Wu, Akihiko Yokoyama, Wiley.
4. Smart Grid: Fundamentals of Design and Analysis by James A. Momoh

References:

1. IEEE papers
2. NPTEL courses

Syllabus for Semester II, M.Tech (Computer Science & Engineering)

Course Code:CST561-1 (Group Elective-I) **Course : Optimization Techniques in Artificial Intelligence**
L:4Hrs,T:0Hr,P:0Hrs, Per Week **Total Credits:04**

Course Outcomes:

On successful completion of the course, students will be able to:

1. Explain how biological systems exploit natural processes.
2. Analyze how complex and functional high-level phenomena can emerge from low-level interactions.
3. Understand how large numbers of agents can self-organize and adapt.
4. Design and implement simple bio-inspired algorithms.

Syllabus:

INTRODUCTION- What is Life? Life and Information, The Logical Mechanisms of Life, What is Computation? Universal Computation and Computability, Computational Beauty of Nature (fractals, L-systems, Chaos) Bio-inspired computing, Natural computing, Biology through the lens of computer science

COMPLEX SYSTEMS AND FUZZY SYSTEMS - Complex Systems and Artificial Life, Complex Networks - Self-Organization and Emergent Complex Behavior, Cellular Automata, Boolean Networks, Development and Morphogenesis, Open-ended evolution, Introduction to Fuzzy Set Theory, Uncertainty and Fuzzy, Hedges and Alpha Cuts, Fuzzification Models, Methods of Defuzzification

NATURAL COMPUTATION AND NEURAL NETWORKS -Biological Neural Networks, Artificial Neural Nets and Learning, pattern classification & linear separability, single and multilayer perceptrons, backpropagation, associative memory, Hebbian learning, Hopfield networks, Stochastic Networks, Unsupervised learning

EVOLUTIONARY SYSTEMS AND ALGORITHMS -Evolutionary Programming: biological adaptation & evolution, Autonomous Agents and Self-Organization: termites, ants, nest builiding, flocks, herds, and schools. Genetic Algorithms!: Schema theorem, Reproduction, Crossover, Mutation operators

COMPETITION, COOPERATION AND SWARM INTELLIGENCE - Collective Behavior and Swarm Intelligence, Social Insects, Stigmergy and Swarm Intelligence; Competition and Cooperation, zero- and nonzero, sum games, iterated prisoner's dilemma, stable strategies, ecological & spatial models, Communication and Multi-Agent simulation – Immuno computing

Text and Reference Books:

1. Leandro Nunes De Castro, Fernando Jose Von Zuben, "Recent Developments in Biologically Inspired Computing", Idea Group Publishing, 2005.
2. Leandro Nunes De Castro, "Fundamentals of Natural Computing: Basic concepts, Algorithms and Applications", Chapman & Hall/ CRC Computer & Information Science Series, 2006.
3. Dario Floreano, Claudio Mattiussi, "Bio-Inspired Artificial Intelligence: Theories, Methods and Technologies", MIT Press, 2008.
4. George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic: Theory and Applications, Prentice Hall, 2005

Websites and External Links

1. http://informatics.indiana.edu/rocha/i-bic/
2. http://web.eecs.utk.edu/~mclennan/Classes/420/
3. http://www.cs.stir.ac.uk/courses/31YB/

Syllabus for Semester II, M.Tech (Computer Science & Engineering)

Course Code:CST561-2 (Group Elective-I) **Course : Social Network Analysis**

L:4Hrs,T:0Hr,P:0Hrs,Per Week **Total Credits:04**

Course Outcomes:

On successful completion of the course, students will be able to:

1. Understand the fundamental principles of social network analysis and applications.
2. Apply network-based reasoning to elicit social policy recommendations.
3. Understand the measures of network composition and structures in social phenomenon.
4. Understand the opportunities and challenges due to pervasive social network data on the internet

Syllabus:

Social network data:

Introduction &What's different about social network data? Nodes, boundaries, Modality Relations , Sampling ties, Multiple, Scales. Why formal methods? Using graphs to represent social relations. Using matrices to represent social relations. Connection and distance, Networks and actors, exchange, Connection ,demographics, Density, Reachability, Connectivity, Distance ,Walks etc., diameter, Flow.

Network centrality:

Density, Reciprocity, Transitivity, Clustering, Krackhardt's Graph Theoretical Dimensions of Hierarchy. Ego networks, Centrality and power, Degree centrality Degree: Freeman's approach, Closeness, Betweenness Centrality

Cliques and Sub-groups:

Groups and sub-structures, Bottom-up approaches ,Top-down approaches, Defining equivalence or similarity ,Structural equivalence, Automorphic, Regular equivalence,
Measures of similarity and structural equivalence

Measuring similarity/dissimilarity:

Pearson correlations covariance's and cross-products, distances, Binary , Matches: Exact , Jaccard , Hamming, Visualizing similarity and distance ,Describing structural equivalence sets :Clustering similarities or distances profiles, CONCOR 37

Automorphic Equivalence:

Defining automorphic equivalence, Uses of the concept, Finding equivalence Sets, All permutations (i.e. brute force), Optimization by tabu search, Equivalence of distances: Maxsim

Small world network models, optimization, strategic network formation and search Concepts:

Small worlds, geographic networks, decentralized search, Contagion, opinion formation, coordination and cooperation, SNA and online social networks

Reference Books:

1. Hanneman, Robert A. and Mark Riddle. 2005. Introduction to social network methods. Riverside, CA: University of California
2. Stanley Wasserman and Katherine Faust; Social Network Analysis - Methods & Applications; Cambridge Univ. press; 1998.
3. John Scott: Social Network Analysis - A Handbook; Second Edition ; SAGE Publication; 2000.
4. CharuAgrawal; Social Network Data Analytics ; Springer; 2011.
5. WouterNooy, Andrei Movar and Vladimir Batagelj; Exploratory Social Network Analysis with Pajek; Cambridge Univ. press; 2005.

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENT599-2 **Course : Digital System Design with FPGA**

L : 3 Hrs., P : 0 Hrs., Per week **Total Credits : 3**

Course Objectives:

The objective of this course is to provide students with

1. Introduction to digital system design flow and approaches.
2. Concept of Hardware description language.
3. Understanding of combinational, sequential, arithmetic circuits & their hierarchical implementation.
4. Knowledge of architecture of Programmable Logic Devices like FPGA

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to :

I. Design and analyze combinational, sequential and arithmetic circuits
II. Understand digital system design flow, timing, synthesis and FPGA implementation issues.
III. solve engineering problems in the area of digital system design.

Basic Digital Systems : Combinational Circuits, Sequential Circuits, Timing.

Digital System Design : Top down Approach to Design, Case study, Data Path, Control Path, Controller behavior and Design, Case study Mealy & Moore Machines, Timing of sequential circuits, Pipelining, Resource sharing.

Hardware Description language : Introduction, Behavioral, Data flow, Structural Models, Simulation Cycles, Process, Concurrent Statements, Sequential Statements, Loops, Sequential Circuits, FSM Coding, Library, Packages, Functions, Procedures, Test bench.

FSM Design : Controller (FSM), meta - stability, synchronization, FSM issues, timing issues, pipelining, resource sharing, case study.

FPGA : FPGA Architecture Xilinx and Altera, Logic block and routing architecture.

Text Books:

1. A VHDL Primer, Third Edition : J. Bhasker, Prentice Hall, (1999).
2. Digital Systems Design Using VHDL, Second edition. Lizy Kurian John, Charles H. Roth, Cengage ; (2012)
3. Fundamental of Digital Logic with VHDL Design, Third Edition, Stephen Brown, Zvonko Vranesic, McGraw Hill Education (2012)

Reference Book :

1. An Engineering Approach to Digital Design : W. Fletcher, Prentice Hall
2. VHDL for Engineers, Kenneth L. Short, Pearson Education (2009)

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : ENP561 **Course : Seminar**
L : 0 Hrs., P : 2 Hrs., Per week **Total Credits : 1**

Course Objectives:
The objective of this course is to provide students with
1. Platform to study contemporary topics in VLSI Design and communicate effectively.

Course Outcomes:
Upon completion of this course, students should demonstrate the ability to
I. Identify the contemporary topic pertaining to VLSI Design.
II. Present the topics with good written and oral communication skills.

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code : ENT651 **Course : System - on - Chip**
L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Objectives:
The objective of this course is to provide students with
1. Understanding of system on Chip architecture and its organization.
2. Introduction to modern embedded processor architectures and Interconnects for SoC Design
3. Fundamental concepts of Network on Chip
4. Knowledge of various aspects of MPSoC
5. Comprehend study of SoC Design flow

Course Outcomes:
Upon the completion of this course, students will demonstrate the ability to :
I. Apply the knowledge of SoC architecture and organization in embedded systems.
II. Explain basic concepts of NoC design by studying the topologies, router design
III. Contribute the knowledge in Multi Processor system on chip design process
IV. Design SoC based Embedded System on FPGA.

Syllabus :
Introduction to the Systems Approach, Chip Basics : Time, Area, Power, Reliability and Configurability, Design Trade - Offs, Requirements and Specifications, Processors : Processor Selection fo SoC, Basic Concepts in Processor Microarchitecutre, Vector, Very Long Instruction Word (VLIW), and Superscalar Processors.
Memory Design : System - on - Chip and Board - Based Systems.
Interconnect : Bust : Basic Architecture, SoC Standard Buses, AMBA, Core Connect, Bus Interface Units : Bus Sockets and Bus Wrappers, SoC Testing
Network - on Chip ; Architecture, Topologies, Switching strategies, Routing Algorithm.
MPSoCs : MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design.
Design of ARM Based SoC, Testing.

Text Books :
1. Computer System Design : System - on - Chip : Michael J. Flynn, Wayne Luk, Wiley India 2012.
2. On-Chip Communication Architectures : System on Chip Interconnect : Sudeep Pasricha, Nikil Dutt, Morgan Kaufmann Publisher, 2008
3. Modern VLSI Design : IP-Based Design, Wayne Wolf, PHI Learning 4/E (English) 4th Edition.

Reference Books :
1. Michael Keating, Pierre Bricaud, "Reuse Methodology Manual for System on Chip Designs", Kluwer Academic Publisher, 2E, 2008.
2. ARM University Program "System - on - Chip " Module

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code : ENT652-1 **Course : VLSI Testing**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Objectives:

The objective of this course is to provide students with

1. Understanding of VLSI design testing issues.
2. Concepts of fault modeling and simulation.
3. Techniques to generate test patterns for faults in a system and design a system for test ability.
4. Knowledge of boundary scan standard and testing techniques for CMOS IC's.

Course Outcomes :

Upon the completion of this course, students will demonstrate the ability to :

I. Identify the different testing issues.
II. Apply knowledge of test - pattern generation and Design for testability techniques for testing of digital systems.
III. Understand boundary scan standard and testing techniques for CMOS IC's.

Syllabus :

Scope of testing : Fundamentals of VLSI testing, verification in VLSI design process. Issues in test and verification of complex chips, embedded cores and SOCs, VLSI Technology Trends Affecting Testing.

Fault modelling : Fault Equivalence, Fault Collapsing, Fault Dominance.

Fault Simulation : Algorithms for Fault Simulation, Serial Fault Simulation, Parallel Fault Simulation, Deductive Faulty Simulation, Concurrent Fault Simulation, IDDQ testing, Delay testing.

Teastability measures : controllability and observability SCOAP

Test pattern generation : D Algorithm, PODEM Algonithm,

Memory Testing : Memory fault model, Stuck at fault, Transition Fault, Coupling Fault, In version Coupling Fault, Idempotent Coupling Faults. Address Decoder Faults. Neighborhood Pattern Sensitive fault, Memory testing Algorithms.

Design for testability : Trade Offs, Adhoc Design for Testability Techniques, Scan design. LSSD, Test interface and boundary scan.

BuilT in Self-Test (BIST) : Test Pattern Generation for BIST, BIST Architectures. MCM Testing. Yield models.

TextBooks :

1. Essentials of Electronic Testing for Digital, Memory and Mixed - Signal VLSI Circuits : M. Bushnell and V.D. Agrawal, Kluwer Academic Publisher, 2000.
2. Digital Systems Testing and Testable Design : M. Abramovici, M.A. Breuer and A. D. Friedman, IEEE Press, 1990.

Reference Books :

1. Introduction to Formal Hardware Verification : T. Kropf, Springer, Verlag, 2000.
2. System - on - a - Chip Verfication Methodology and Techniques : P. Rashinkar, Paterson and L. Singh, Kluwer Academic Publisher, 2001.

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code : ENT652-2 **Course : Nanoelectronics**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Objectives:

The objective of this course is to provide students with

1. Understanding of contemporary relevance and potential of nanoelectronics
2. Knowledge of how factors like scaling and dimension lead to novel behaviour of nanoelectronics components.
3. A comprehensive understanding variety of nanoelectronics phenomena, nanoelectronics components and their possible applications.

Course Outcomes :

Upon completion of this course, students will demonstrate the ability to :

I. Show a deeper understanding of the relation between novel behaviour of nanoelectronics devices and quantum behaviour of matter at the nano scale as well as the breakdown of received scaling wisdom
II. Appreciate scaling issues and ideas behind nanoscale fabrication technologies.
III. Understand the Principles of devices such as tunneling diodes, single electron tranisistor, spintronic devices.

Syllabus :

Introduction to Nanoelectronics, Shrink-down aproaches, CMOS Scaling, challenges and future .

Classical particles, classical waves and quantum particles, Quantum mechanics of electons

Single Electron and Few Electron phenomena and Devices: Tunnel junctions and applications of tunneling, Coulomb Blockade and the single electron Transistor, Other SET and FET structures.

Many Electron Phenomena : Particle statics and density of states, Quantum Wells, Quantum Wires and Nanowires, Quantum Dots and Nanoparticles

Fabrication Techniques for nanostructures

Ballistic transport and spin transport, Carbon nanotube and Nanowires, transport of spin and spintronics devices and applications.

Text Books :

1. Fundamental of Nanoelectronics, first Edition, George W. Hanson, Pearson education, prentic Hall, 2008

Reference Books :

1. Nanosystem, K. E. Drexler, Wiley 1992
2. Introduction to Nanotechnology, C.P. Poole Jr., F.J. Owens, Wiley 2003

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code : ENT652-3 **Course : Low Power VLSI Design**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Objectives:

The objective of this course is to provide students with

1. Understanding of sources of power consumption of CMOS circuits
2. Understanding of Power Reduction Techniques and Low Power Logic design Styles.

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to :

I. Analyze the power consumption of CMOS circuits
II. Design low - power CMOS circuits using various strategies at different design levels.

Syllabus :

Introduction : Advances in IC technologies, Design challenges in deep submicron MOS. Power dissipation. Power density. Supply voltage scaling. Scaling impact on supply current. Supply voltage scaling impact on delay. Power consumption and battery capacity trends. Power sources for low-power devices. Classes of batteries, battery types classification of application.

CMOS Power Consumption Sources, Capacitance in a CMOS circuit, Dynamic Power Reduction Techniques: transition probability minimization, glitch reduction, supply voltage reduction, clock gating, multi-supply design, dynamic voltage and frequency scaling. Clock gating. Multi-supply design: multiple VDD considerations, optimum numbers of supplies, dual - supply inside a logic block, level shifters, distributing multiple supply voltage : conventional and shared-well.

Power Reduction Techniques : multiple threshold, transistor stacking, input vector control, sleep transistor, variable threshold technique. Multiple threshold technique, dual threshold CMOS, using multiple thresholds. Transistor stacking, self-reverse biasing, leakage control stacking. Input vector contol : influence on subthreshold, gate, BTBT and total leakage. Sleep transistor technique. Low power sensor networks.

Low Power Logic Styles : Advantages and disadvantage of static CMOS. Low-power logic styles, Logic activity. Charge leakage. Problems with dynamic CMOS. Domino Logic. Selecting a logic style. Adiabatic Logic. Power saving and energy recovery. Charging with constant current, charge in N steps. Adiabatic dynamic CMOS inverter, Quasi-Adiabatic Logic. Technology distribution, Power and area analysis.

Text Books :

1. Low Power Digital CMOS Design. I edition. 2008 : Chandrakasan. R. Brodersen. Springer
2. Low-Power CMOS Circuits : Technology, Logic Design and CAD Tools : C. Piguet CRC. 2005.
3. Low-Power Digital VLSI Design: Circuits and Systems : A. Bellaouar, M. Elmasry Springer : 1 edition. 2006

Reference Books :

1. CMOS/BiCMOS VLSI : Low Voltage, low Power : K.S. Yeo, S.S. Rofail, W.L. Goh. - Prentic Hall, 2002.
2. Low - Power CMOS VLSI Circuit Design : K. Roy, John Wiley & Sons Inc., 2003

SYLLABUS OF SEMESTER III, M. Tech. (VLSI DESIGN)

Course Code : ENP653 **Course : Project Phase - I**

L : 0 Hrs., P : 3 Hrs., Per week **Credits : 6**

Course Objectives:

The objective of this course is to provide students with

1. An assistance to understand and solve engineering porblems in industry and research.
2. Understanding to apply techniques, skills, and modern EDA tools to identify, formulate and solve the engineering problems.
3. Understanding to analyze research outcome and communicate it in effective manner with understanding of ethical, social and legal practices in profession.

Course Outcomes :

Upon completion of this course, students will demonstrate the ability to :

I. Critically evaluate alternate assumptions, approaches, procedures, tradeoffs, and results related to engineering problems.
II. Apply engineering knowledge for design and implementation of VLSI based circuits and systems in an ethically responsible manner.
III. Use written and oral communications to document the research work and present results.
IV. Engage in self & life - long learning in continuing professional development.

Course Assessment

The final grade will be determined using the following scheme :

a. Internal Assessment :- 50 Marks

Internal assessment is carried out twice of total 25 marks by a panel of internal examiners. Continuous project evaluation is also carried out by concerned guide which carries 25 Marks. Thus overall evaluation for 50 Marks is carried out as continuous internal evaluation process.

b. External Assessment : 50 Marks

External Assessment is carried out by External Examiner to review the progress of project work.

SYLLABUS OF SEMESTER IV, M. Tech. (VLSI DESIGN)

Course Code : ENP654 **Course : Project Phase - II**

L : 0 Hrs., P : 6 Hrs., Per week **Credits : 12**

Course Objectives:

The objective of this course is to provide students with

1. An assistance to understand and solve engineering problems in industry and research.
2. Understanding to apply techniques, skills, and modern EDA tools to identify, formulate and solve the engineering problems.
3. Understanding to analyze research outcome and communicate it in effective manner with understanding of ethical, social and legal practices in profession.

Course Outcomes :

Upon completion of this course, students should demonstrate the ability to :

I. Critically evaluate alternate assumptions, approaches, procedures, tradeoffs, and results related to engineering problems.
II. Apply engineering knowledge for design and implementation of VLSI based circuits ad systems in an ethically responsible manner.
III. Use written and oral communication to document the research work and present results.
IV. Engage in self & life - long learning in continuing professional development.

Course Assessment

a. Internal Assessment : 150 Marks

Internal assessment is carried out thrice for total 100 marks by a panel of internal examiners. Continuous project evaluation is also carried out by concerned guide which carries 50 Marks. Thus overall evaluation for 150 Marks is carried out as continous internal evaluation process.

b. External Assessment : 150 Marks

External Assessment is carried out by External Examiner after the successful completion of project work.

SHRI RAMDEOBABA COLLEGE OF ENGINEERING AND MANAGEMENT, NAGPUR

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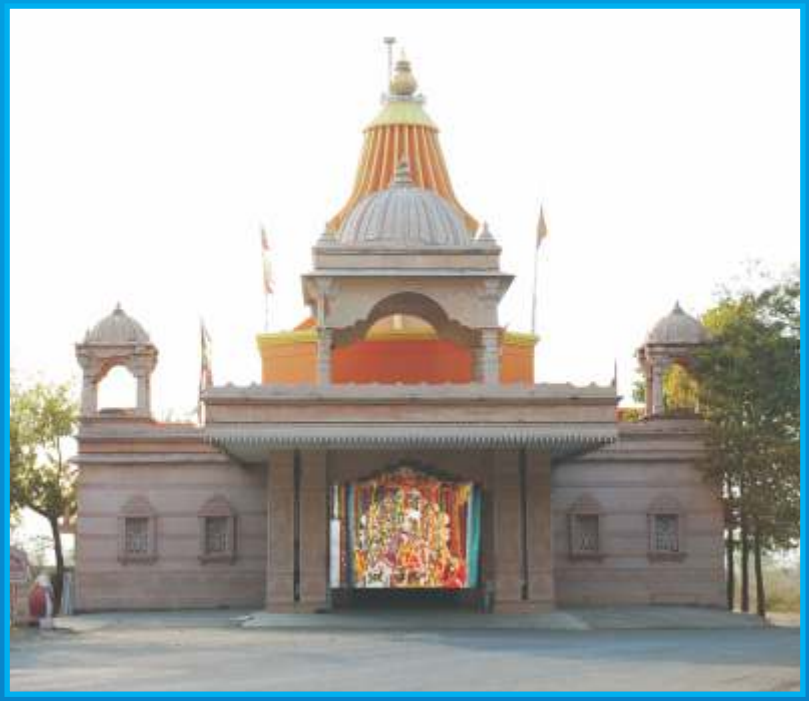

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