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Technical Report

Reliability Characterization of MEMS Cantilever Switch

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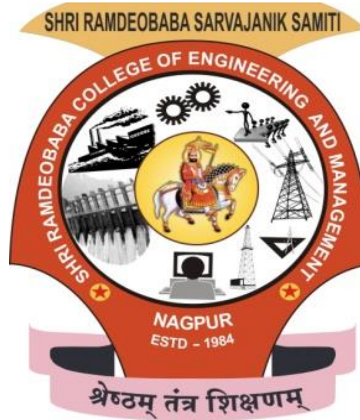

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1. INTRODUCTION

Microcantilever switches have demonstrated superior characteristics compared to FET and diode based structures. However before this technology can be inserted into mainstream systems, adequate reliability and lifetime issues of these electromechanical devices must be demonstrated. The long-term reliability of microcantilever switches is of major concern and is currently the subject of investigation. One of the factors limiting implementation of MEMS switches is the limited switch lifetime. There are several problems reported to affect the lifetime of MEMS switches, such as creep in the metal cantilever, distortion in the nominal air gap, and stiction of the metal membrane to the dielectric layer [1][2]. The stiction is a major cause of failure. The stiction depends on dielectric charging which is related to actuation voltage. The exact physics of dielectric charging is not fully understood today. A simple but unsubstantiated theory of dielectric charging envolves the concept of charge tunnelling into the dielectric which in term affect the actuation voltage of the switch.

The nominal air gap height between the membrane and the dielectric surface might be distorted by surface roughness of the contacts, or residue left after the releases etch [3]. The change in nominal air gap height degrades the on/off capacitance ratio and increases the pull-down voltage. The performance of the switch is believed to be affected by surface roughness of the deposited dielectric. It was reported that, with the change in surface roughness value, the on-off capacitance ratio of Si_3N_4 films may change to approximately 40% of their actual values [4]. Therefore, it is necessary that the surface roughness of the dielectric layer must be studied. When switch is actuated, a high electrostatic field across the thin dielectric layer causes charges to build up in the dielectric [5]. These charges hold the cantilever either fully (failing the switch completely) or partially (degrading the Con/Coff ratio) in the down position when the voltage is removed [6]. Consequently, the metal cantilever can't be released unless enough time is given for the charges to relax in the system. This process can last on the order of long time depending upon the dielectric material [5][6]. This effect is manifested as a shift of the Current – voltage (I-V) curve with time and cycling [7]. The real nature of the charge trapping in the dielectric of cantilever switches is not currently identified [8]. For long term reliability and operation of these devices, the detailed analysis and testing is essential.

In MEMS Cantilever Switch when the Control voltage is applied to the bottom electrode, the membrane in contact with the dielectric forms a large capacitor. To characterize the trap state of the dielectric, charging and discharging transient, measurement on the switch whose membrane was intentionally fabricated in the permanently down position is considered. This resembles to a Metal- Insulator- Metal capacitor. The dielectric charging depends on electric field. The second order effect such as roughness of the surface also affects the electric field. Hence to study these effects fabrication, characterization of MIM test structure is carried out. The evaluated MIM results needed to be correlated with MEMS Cantilever Switch. Process to fabricate microcantilever switch has been developed and device has been successfully fabricated with surface micromachining technique. The through electrical characterization of microcantilever switch is carried out to verify the functionality and to study the reliability issues of the device.

2. MICROCANTILEVER SWITCH

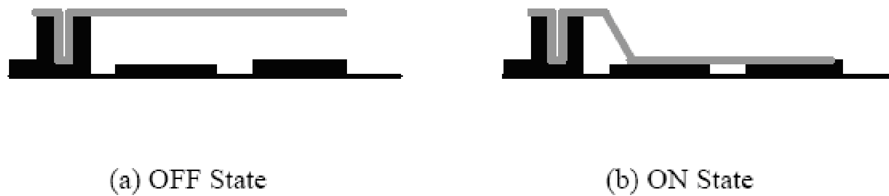


Fig. 1. Microcantilever Switch (ON and OFF state).

A typical Microcantilever used for switching application consists of a cantilever as actuating element to make the contact between the two metal terminals of the switch shown in Fig.1. MEMS switches can be electrostatically actuated i.e. When voltage is applied to the electrodes, the electrostatic force acting on the electrodes pull down the cantilever beam toward the ground making the switch ‘ON’ and when the applied voltage is removed, the membrane returns back to its normal position making the switch ‘OFF’.

Since in the closed state the MEMS capacitive switch is similar to a MIM capacitor [9] [10]. Test structure to identify the charging effect is nothing but the MIM capacitor. The origin of stiction is charge trapping in dielectric is studied with the help of MIM test structure. We intend to minimize this effect through our study.

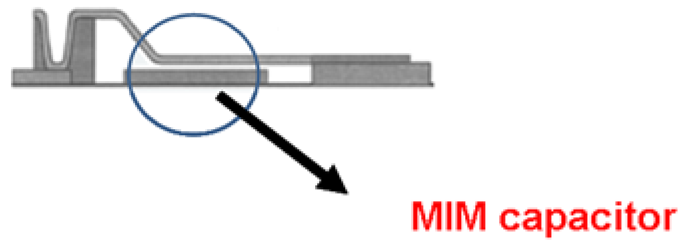


Fig. 2. MIM Capacitor test Sructure

3. FABRICATION OF MIM TEST STRUCTURE

For MIM capacitor fabrication, Aluminium is used for top and bottom electrodes and Silicon Nitride is used as dielectric layer. An oxide layer was grown on wafer to isolate the bottom metal from the substrate. The silicon nitride film was deposited by two different deposition methods. The ICPCVD silicon nitride film was deposited at room temperature and the HWCVD silicon nitride film was deposited at three different temperatures on different silicon wafers to obtain three different surface profiles for the given HWCVD deposition system. For device fabrication and characterization facilities available at IIT, Bombay is avail under INUP program [11]. The Detailed fabrication flow is described below

The fabrication of MIM test devices required various processing step such as cleaning of the wafer, film deposition and film patterning. The test structures have been fabricated on P-type 10 - 100 Ωcm <100> Silicon wafer. The wafers were first cleaned and then oxide was grown over it. Then bottom aluminum, silicon nitride and top aluminum layers have been deposited. To pattern top metal and make bottom metal contact lithography was done.

Schematic stepwise process flow is shown in Fig.3.

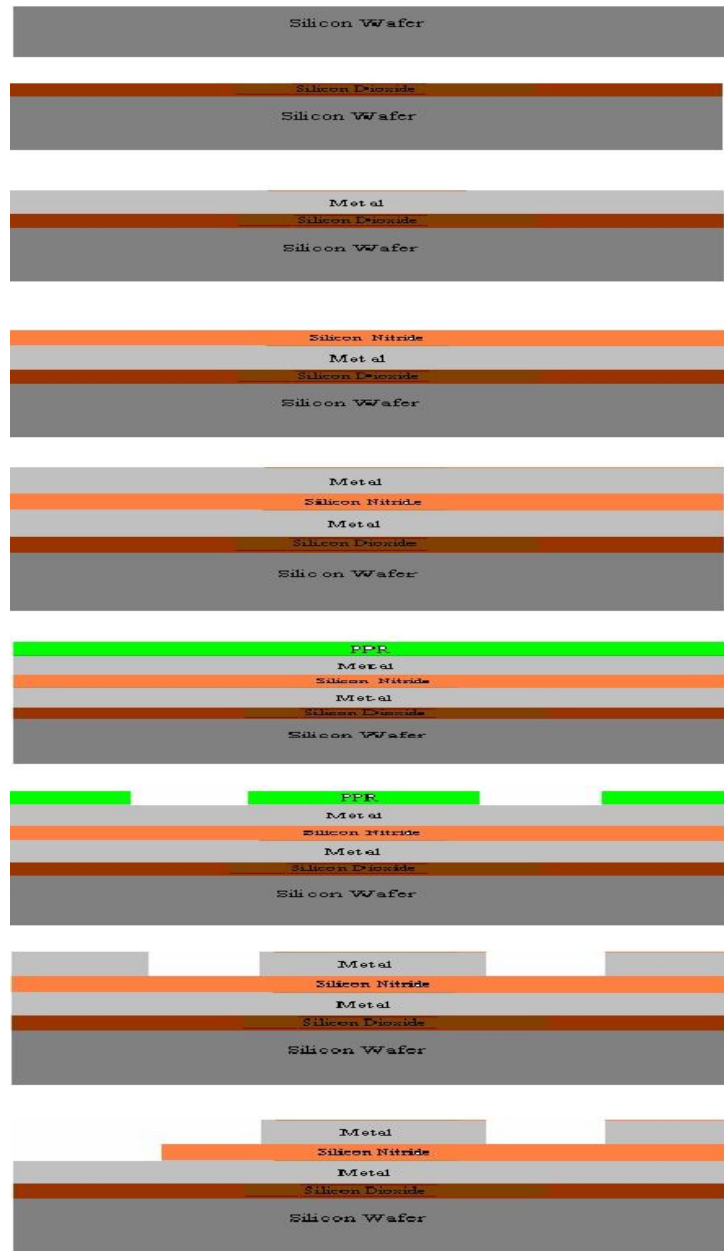


Fig.3. Schematic stepwise process flow for MIM Test Structures

The process details are as follows.

Wafer specification - p-type <100>, 1-10 Ωcm

1. **RCA cleaning**
2. **Dry Oxidation - 100 nm thickness**
3. Metal deposition by e-beam evaporation: Al thickness - 100nm
4. Silicon nitride deposition by HWCVD (at different temperature) & ICPCVD, Si_3N_4 thickness - 100 nm, At room Temperature, 4.1mtorr
5. Metal deposition by evaporation: Al thickness - 100nm thickness
6. Lithography for top metal patterning: Optical lithography
7. Aluminum etching
8. Removal of unexposed PPR
9. Lithography for Si_3N_4 patterning
10. Silicon nitride etching to make bottom metal contact: using RIE

Mask used in lithography process is shown in Fig. 4.

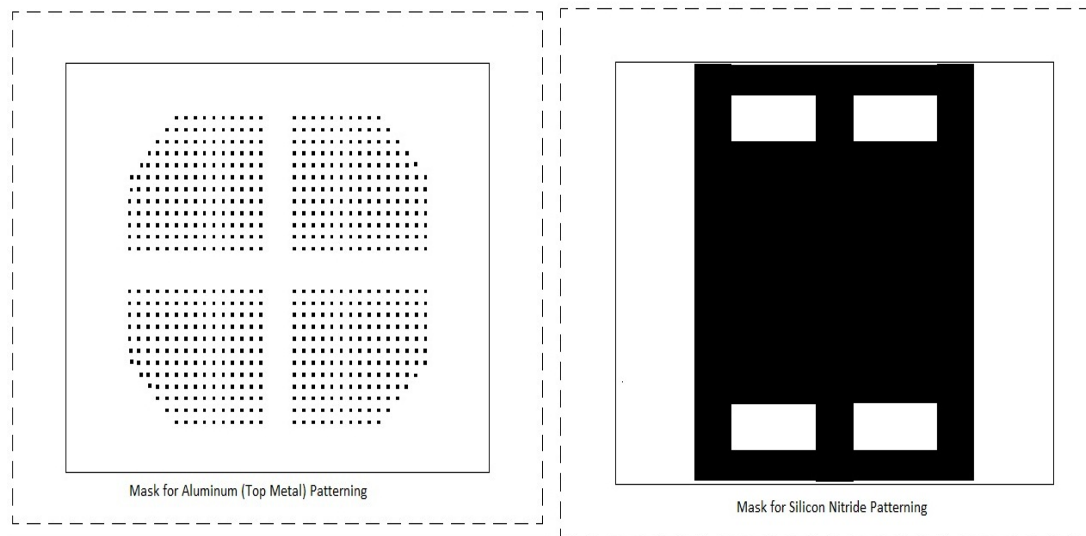


Fig. 4. Mask design for two masking levels.

Fabricated MIM devices are shown in Fig.5.

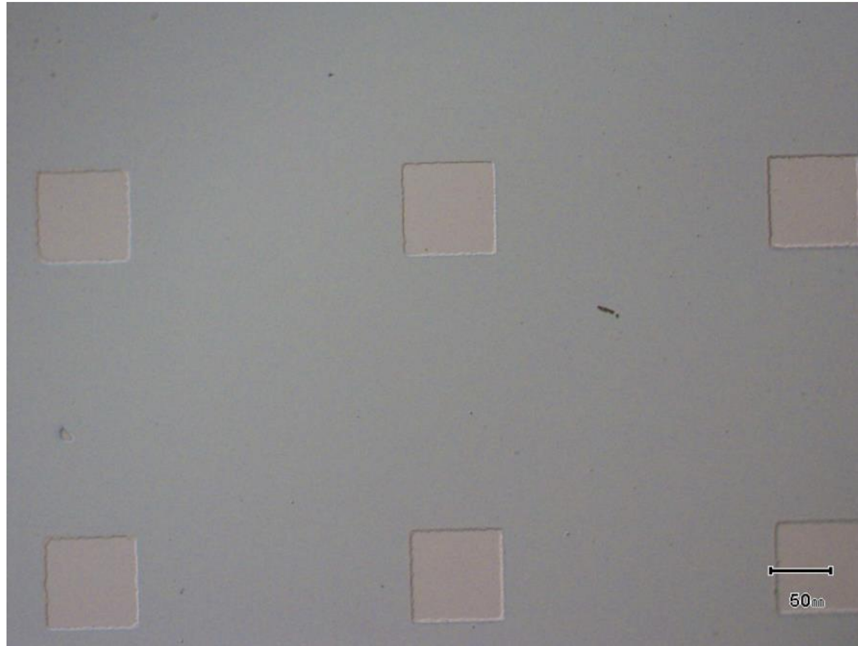


Fig.5. Fabricated MIM Capacitor

3.1 FABRICATION PROCESS DETAILS

P type wafer <100> orientation of high resistivity which allows the possibility for integration with CMOS for multifunction assemblies say more than 10Ωcm is used for fabrication.

1) Wafer cleaning→ Radio Corporation of America (RCA) cleaning has been done to remove the contaminants from wafer. RCA removes organic contaminants (such as dust particles, grease or silica gel) from the wafer surface; then removes any oxide layer that might have built up and finally, removes any ionic or heavy metal contaminants. It is a standard set of wafer cleaning steps which needs to be performed before any high temperature process. RCA cleaning is a two steps process:

SC 1 - standard clean 1 is done to remove organic contaminants. After SC 1, HF dip is given to the wafer to remove the oxide layer that might have been formed during this process.

SC 2 - standard clean 2 is done to remove the traces of metallic contaminants.

SC 1 →	180 ml DI water + 25 ml NH_4OH at 70°C, 5min
	Add 50 ml H_2O_2 and heat for 6 - 8 min
	Allow wafer to cool for 10 - 20 min
	DI water dip, 30 sec HF dip, DI dip
SC 2→	180 ml DI water + 25 ml HCl at 70°C for 5 min

Add 50 ml H_2O_2 and heat for 3 - 6 min

Allow it to cool for 10 - 12 min

DI water dip, 30 sec HF dip, DI dip.

RCA cleaning wet bench is shown in Fig. 6.

RCA cleaning bench:

- RCA chemicals used: DI water, NH_4OH, H_2O_2, HCl, HF
- Piranha chemicals used: H_2SO_4, H_2O_2
- HF cleaning: 2% HF
- Substrates used: Si, glass.
- Substrate size: Max 4" diameter wafer.

Fig. 6. RCA cleaning wet bench

2) Thermal oxidation (SiO_2)

Oxidation of the wafer is done to improve isolation between devices and provide protection against any implant and diffusion. An oxide layer of 100 nm has been grown over RCA cleaned silicon wafer using thermal oxidation process. Oxidation of silicon slice can be carried out by subjecting it to oxygen or water vapour, while it is maintained at elevated temperature.

Process recipe:

- SiO_2 thickness - 100 nm
- Wafer temperature - 1100°C
- Time - 45 min

Furnace 2 is used for thermal oxidation shown in Fig.7.

Furnaces 2:

- **All tubes can handle 2 inch wafers**
- **Pyrogenic oxidation furnace** - Temperature up to 1150^{0} C – gases H_2 and O_2
- **Double walled furnaces**: Uniform growth of oxide – only dry oxidation of silicon wafers
- Solid source dopant and spin on dopant. Max. temp. is 110^{0}C, gases used: O2, H2 & N2

Fig.7. Furnace 2

3) Aluminium deposition.

Process recipe:

- Thickness: 100 nm.
- Metal weight: ~100mg.
- Chamber pressure: 4.3 x 10^{-6} torr.
- Flash Deposition technique employed.

Thermal evaporator is used for aluminium deposition shown in Fig.8.

Thermal Evaporator:

- **Wafer size:** 2 Inch at a time 2-3 wafers can be processed if required
- **Number of current sources to head the filament:** two
- **Number of filaments that can be fitted in the system:** two
- **Material:** Al
- **Base pressure**: 8 X 10-5 mbar
- **Substrate temperature**: Room temperature
- **Coolant required**: Liquid Nitrogen
- **Additional facility**: Shadow masks of 1mm diameter available for making MOS capacitors.

Fig.8. Thermal Evaporator

4) Aluminium patterning

Photolithography is done to pattern the layers of the device. It is process of transferring geometric shapes/patters on a mask to the surface of silicon wafer. It uses optical properties of photosensitive materials to transfer patterns on the desired surface.

Process recipe:

- Dehydrate - 110°C for 30 mins.
- PPR coating - 500 rpm for 10 sec, 3000 rpm for 30 sec
- Prebake (soft bake) - 90°C for 2 min
- Mask alignment.
- Exposure – 7-8 sec UV exposure.
- Development – MF319, 30 to 45 sec.

- Post Prebake (hard bake) - 90°C for 2 min
- Removal of unexposed PPR by Acetone after etching.

For lithography used in Double Sided mask Aligner is used shown in Fig. 9.

Specifications of the system:

- **Exposure modes:** hard, soft, vacuum contact
- **Separation distance:** 0-300 microns
- **Wafer thickness**: 0.1-10 mm
- **Lamp:** 500W Hg Lamp
- **Wavelength range**: 350-450 nm
- **Alignment accuracy:** 0.5 micron for top side and 1 micron for bottom side
- **Minimum feature size achievable:** 2 micron

Process Capabilities:

- **Substrates used**: Silicon, glass
- **Mask plate size:** 3”, 5”
- **Substrate size**: 2”, 4”, quarter of a 2” wafer
- **Gases used**: GN2
- **Positive resist used**: Shipley’s S1813 and S1805

Fig.9. Double Sided mask Aligner (DSA)

5) Silicon Nitride deposition Using HWCVD & ICPCVD

i) Deposition using HWCVD

The dielectric silicon nitride here was deposited using Hot Wire Chemical Vapor Deposition technique. In this technique, the wafer is held at different temperature and the gases react at different temperature. That is the reaction between gases takes place at high temperature to increase reaction rate and the substrate is held at lower temperature so as to allow deposition of over films with less melting temperatures.

In this deposition system we have maintained three different substrate temperatures during deposition of Silicon Nitride films to obtain three different surface profiles of the Silicon Nitride such that we are able to study the effect of surface roughness on performance of dielectric.

The process parameters are -

Silicon Nitride thickness - 100 nm

Filament temperature - 1850°C

Silane: Ammonia ratio - 1:20

It was observed that the deposition rate of silicon nitride changes with change in substrate temperature. So deposition rate at each temperature was calculated by measuring the film thickness deposited over a known time period.

Table 1.Variation of Deposition Time for different deposition temperatures

Sr. No.	Substrate Temperature	Deposition time
1	300ºC	9 minutes
2	200ºC	7 minutes
3	100ºC	5Minutes

Silicon Nitride is deposited using hot wire CVD device shown in Fig. 10

HWCVD:

- ***Make and Model:*** *The system was designed and assembled at IIT Bombay*
- ***Process Capabilities:***
- ***Substrate Size:*** *2 Inches, small pieces of wafer- Si and glass.*
- ***Type of depositions:*** *intrinsic polysilicon, Boron doped polysilicon, silicon nitride.*
- ***Substrate Temperature:*** *Room temperature to 800°c.*
- ***Filament Temperature:*** *Up to 2000 °C.*
- ***Process Gases used****: Silane (SiH4), Ammonia (NH3), Hydrogen (H2), Diborane (B2H6), Nitrogen (N2).*
- ***Chamber Base Pressure****: Up to 10e-7 mbar.*
- ***History of the substrate:*** *Silicon wafers, Glass substrate, wafers coated with SU8, oxide deposited wafers.*

Fig.10. HWCVD System

ii) Using ICPCVD System

The silicon nitride films, with a thickness of 100 nm, were also deposited with the Inductively Coupled Plasma Chemical Vapour Deposition (ICP-CVD) system using a $SiH_4/N_2/Ar$ mixture. The flow rates of SiH_4, N_2 and Ar were fixed at 13.5, 11, and 40 sccm, respectively. The deposition was carried out at room temperature (28°C) and the chamber pressure was maintained at 3.1mtorr. A summary for this deposition can be given as-

Silicon Nitride thickness - 100 nm

Process temperature - 25°C

Silane: Nitrogen: Argon ratio – 13.5:11:40 sccm

RF Power- 40W

ICP Power- 1000W

Chamber Pressure- 3.1mtorr

Deposition Time- 5 minute 30 second

Fig 11. ICPCVD System

Process Capabilities:

- **Types of depositions:** Silicon dioxide, Silicon nitride, silicon oxynitride, and amorphous silicon.
- **Types of substrates:** 2”, 4”, 8”, small pieces of wafers - Si and glass.
- **Substrate History:** Metal coated wafers need to be discussed before processing.
- **Temperature of substrate:** Room temp to 350 °C
- **Process gases used:** Silane for Si_3N_4, SiO_2, SiO_xN, a-Si Nitrogen for Si_3N_4, SiO_xN Nitrous oxide for SiO_2, SiO_xN Ammonia for Si_3N_4 Argon for Plasma CF_4/O_2 for Plasma clean gas
- **Load lock chamber vacuum:** 10e-3 Torr
- **Process chamber vacuum:** 10e-6 Torr

4. CHARACTERIZATION OF MIM TEST STRUCTURE

Physical and electrical characterization of thin film MIM capacitor test structures is carried out. We have measured the surface characteristics of the deposited layer with the help of Atomic Force Microscopy (AFM). After getting an estimate of the surface profiles of the deposited layers electrical characterization of all the devices was done.

4.1 PHYSICAL CHARACTERIZATION

The surface roughness parameters such as average roughness (Ra) or root mean square (rms) roughness can be obtained from AFM. The observations of surface roughness for the deposited dielectric films, measured with atomic force microscopy are as below-

Observation for silicon oxide and bottom metal layer:

The roughness details analysed for the silicon oxide and bottom metal layer for a scan area of 5µm is observed to give RMS surface roughness of 3.49 nm and 4.45nm respectively. The Fig.12. and Fig.13. shows the analysed data for given oxide and metal layer.

The surfaces oxide and bottom metal is imaged using contact mode AFM to investigate how the surface roughness of the previous layer is carried forward by the subsequent silicon nitride layer. The observed values for both the films are low considering the thickness of 100nm.

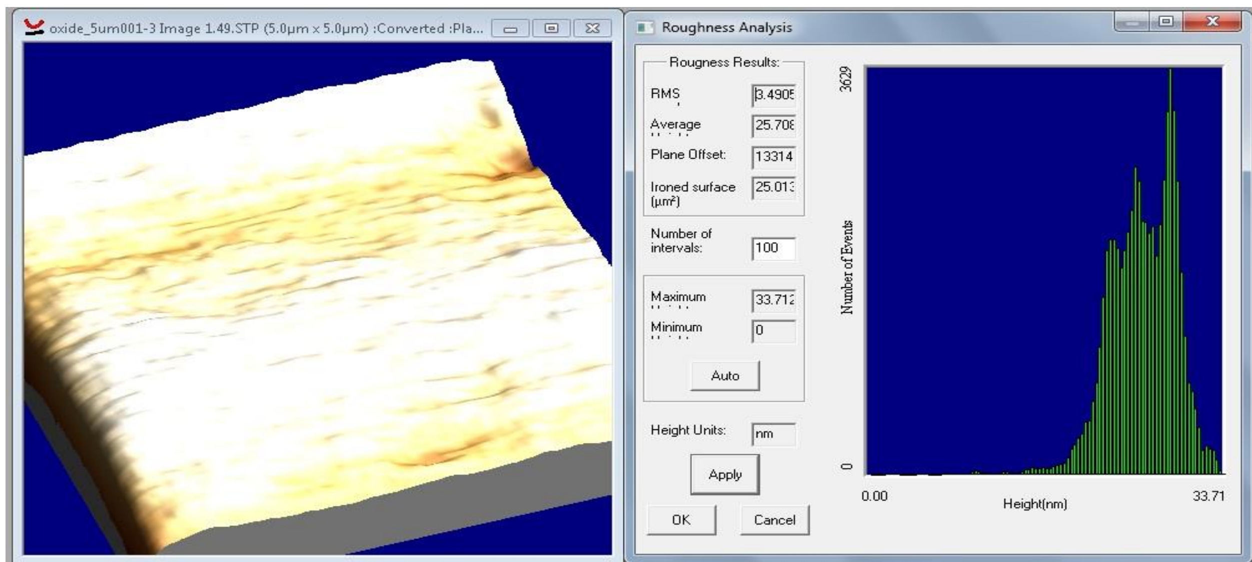


Fig.12. Surface Roughness for Silicon Oxide layer

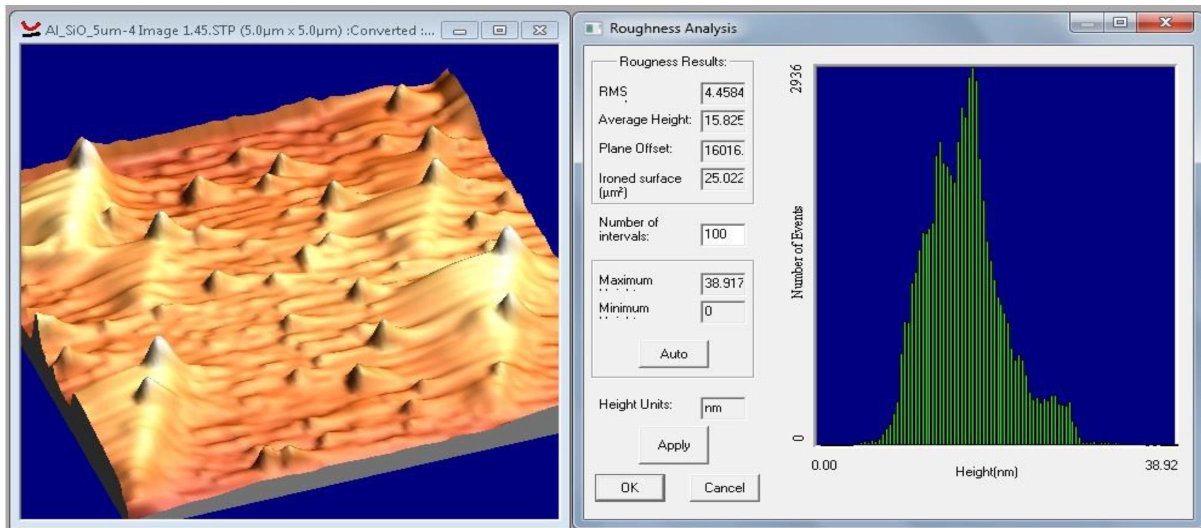


Fig.13. Surface Roughness for Bottom Metal layer

Even though metal deposition through thermal evaporation is very uniform process for a well maintained chamber parameters the observed value of metal layer roughness may be due to the effect of non uniformities of silicon oxide layer beneath it. Next we imaged Silicon Nitride layers for RMS roughness value. These measurements yielded some interesting observations.

Observations of Silicon Nitride Films-

The observations for the performed measurements of RMS surface roughness are summarised as below-

i. HWCVD-300 °C Deposition(3µm scan Area)

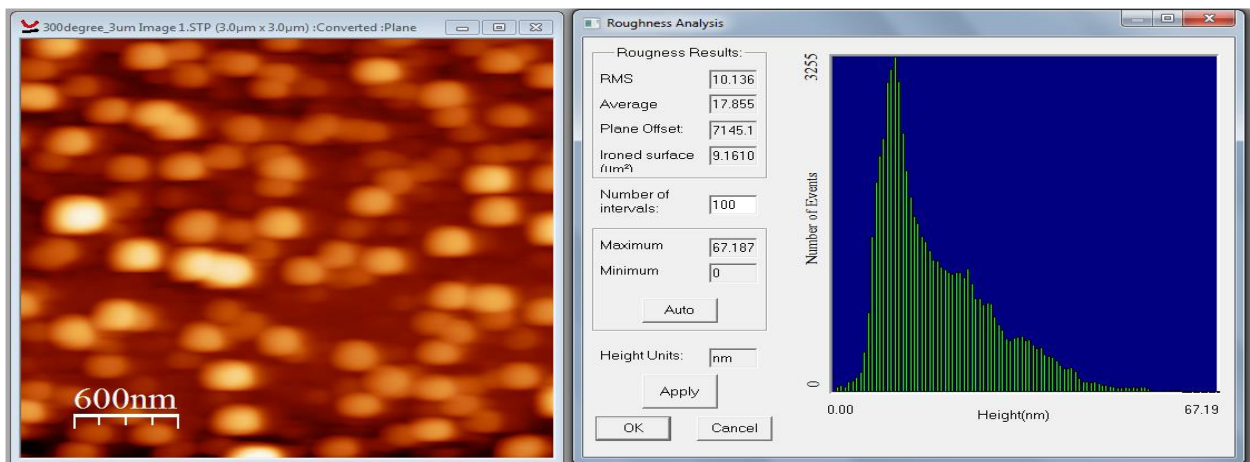


Fig.14. Surface Roughness for Silicon Nitride layer (HWCVD-300 °C)

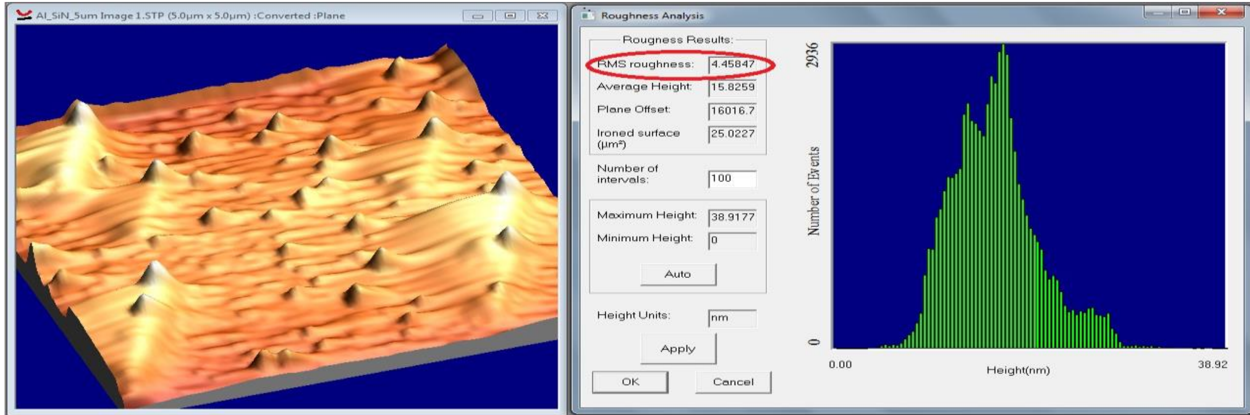


Fig.15. Surface Roughness for Silicon Nitride layer (ICPCVD)

Table 2. Summary of the effect of deposition conditions on the value of surface roughness

Type of Film	Scan Area	RMS Roughness
HWCVD 100 °C Deposition	3µm	4.495 nm
HWCVD 200 °C Deposition	3µm	7.603 nm
HWCVD 300 °C Deposition	3µm	10.136 nm
ICPCVD Room Temp Deposition	5µm	4.458 nm

It was observed that the ICPCVD films show more uniform nature as compared to HWCVD films (Even on scanning over a larger scan area). The surface uniformity of HWCVD films is found to decay with increase in substrate temperature during deposition. The table 2, summarises the effect of deposition conditions on the value of surface roughness. In the table.2, it can be observed that the HWCVD films show high surface roughness value as we consider higher deposition temperature for these films. With all the data available for the film surface topography we proceeded for electrical characterization of the fabricated Test Structures.

4.2. ELECRICAL CHARACTERIZATION

Electrical characterization set up used for testing and measurement of microcantilever is shown in Fig.16.

Fig. 16. Electrical characterization setup

These test structures were characterized for electrical characterizations along with the effect of change of dielectric deposition methods and variations in deposition parameters is as shown below:

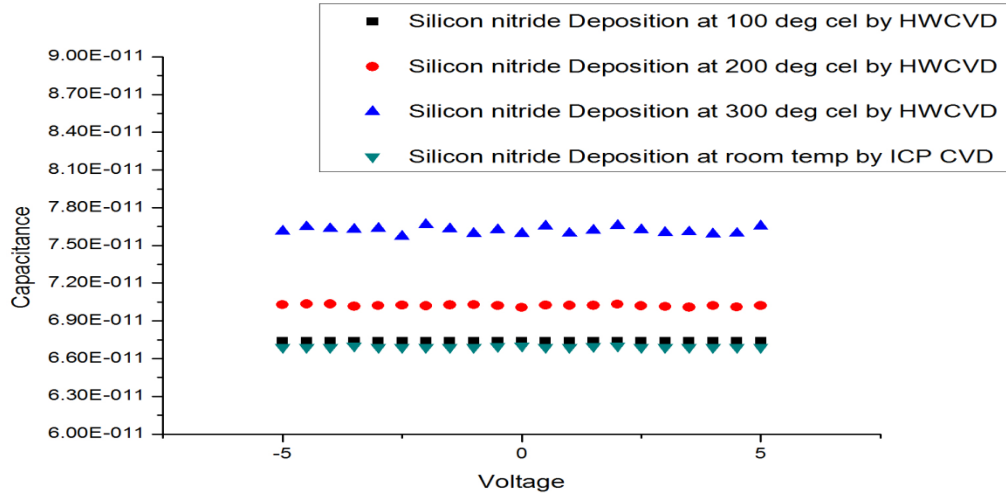
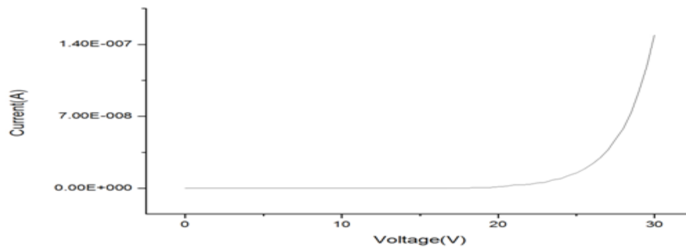


Fig. 17. C-V Characterization

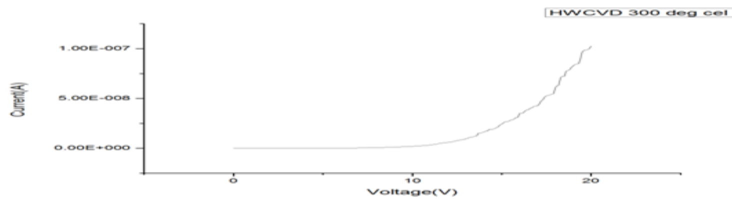
The change in capacitance is correlated with the surface roughness of silicon nitiride which changes with the change in deposition conditions as given in table 2.

The response of leakage current for all the fabricated devices for different electrical fields are shown in below graphs:

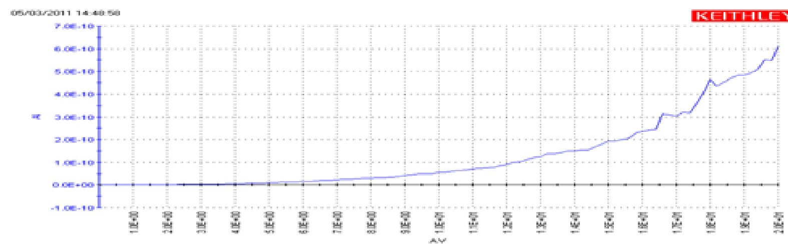
IV of ICPCVD Device



IV of HWCVD Device- 300 deg cel Silicon Nitride



IV of HWCVD Device- 200 deg cel Silicon Nitride



IV of HWCVD Device- 100 deg cel Silicon Nitride

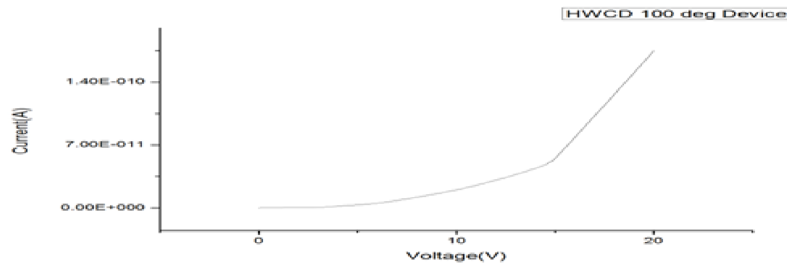


Fig. 18. I-V Characterization

Here for ICPCVD Device we can observe that device show very small leakage current up to 25-26volt but at higher electric field the leakage current starts increasing exponentially with the increase in applied voltage.

Similarly for Si_3N_4 deposited by HWCVD method at 100^0C, 200^0C, 300^0C Current -Voltage (IV) characterization is carried out we observed that ICPCVD deposited devices can withstand higher electric field and provide low leakage current.

For device reliability we require to know the break down points of all the dielectric films, so the films were characterized for breakdown as shown in table 3.

Table.3. Breakdown Voltage for HWCVD and ICPCVD films

Sr. No.	**Type of Film**	**Breakdown Voltage (V)**
1	HWCVD 300 °C Deposition	21V
2	HWCVD 200 °C Deposition	26V
3	HWCVD 100 °C Deposition	29V
4	ICPCVD Room Temp Deposition	37V

The breakdown field for ICPCVD films is much higher as compared to HWCVD films. It takes even more than 20% of maximum observed value of breakdown voltage available for HWCVD films to break the given ICPCVD film. Thus we look forward for ICPCVD films as an emerging candidate to be employed in MEMS cantilever switch fabrication due to its high breakdown strength.

The devices were tested for different stress conditions. The shifts in IV curves were analyzed to study the phenomenon of charge trapping in dielectric on application on constant stresses. The results from constant voltage and current analysis are as shown below:

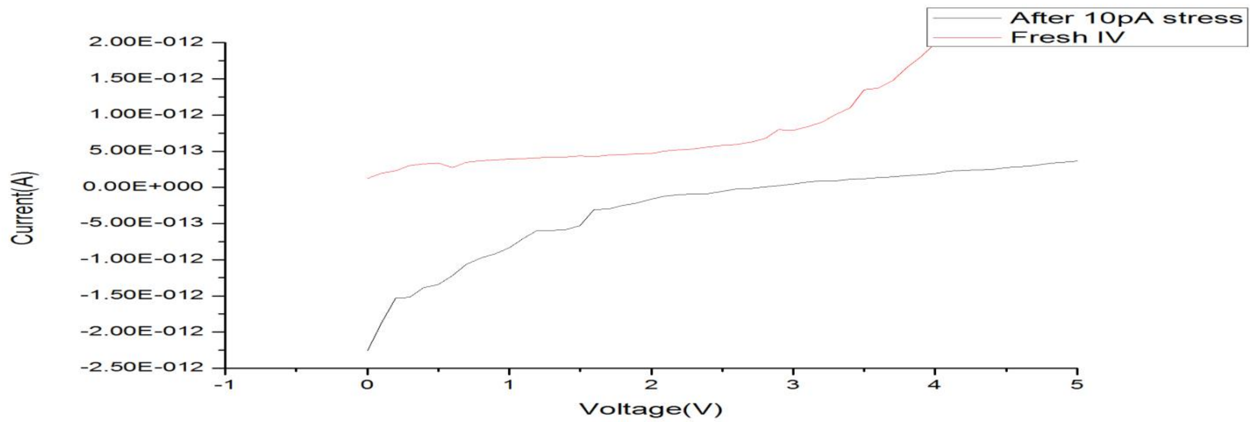


Fig. 19. Constant Current Stress and Corresponding IV shift.

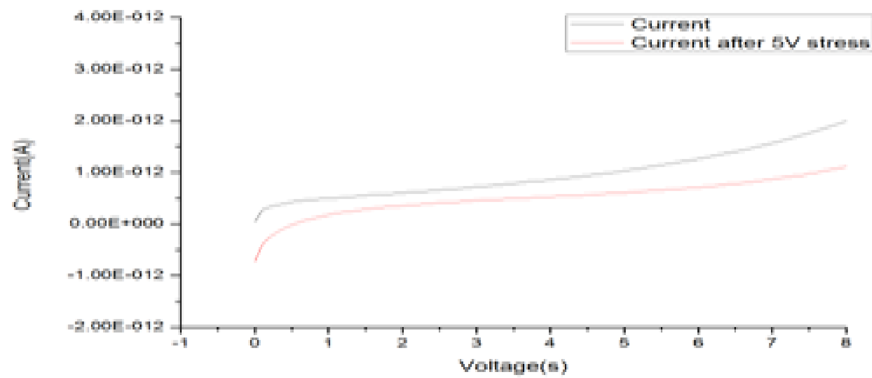


Fig. 20. Constant voltage stress and corresponding I-V Shift

Stressing of test structures is associated with shift in Current-Voltage (IV) characteristics of device. These shifts are proportional to the density of trapped charges. The trap density increases with increase in magnitude of applied stress. For applied stress (Constant Positive Voltage), we observed downward shift in current. The maximum current corresponding to trapped charge after stressing was observed in range of few Pico-amperes. The charges corresponding to this magnitude of current are sufficient to introduce significant shifts in the operating parameters of the device. Stressing of device reduces the strength of dielectric. An indication of this effect is early breakdown of stressed devices. Hence it can be concluded that stressing produces defects which degrade the dielectric strength.

5. FABRICATION OF MICROCANTILEVER SWITCH

The MEMS switches are fabricated using the surface micromachining methods, which is incorporate for level lithography process.The process flow used for fabrication of microcantilever switch is as shown below:

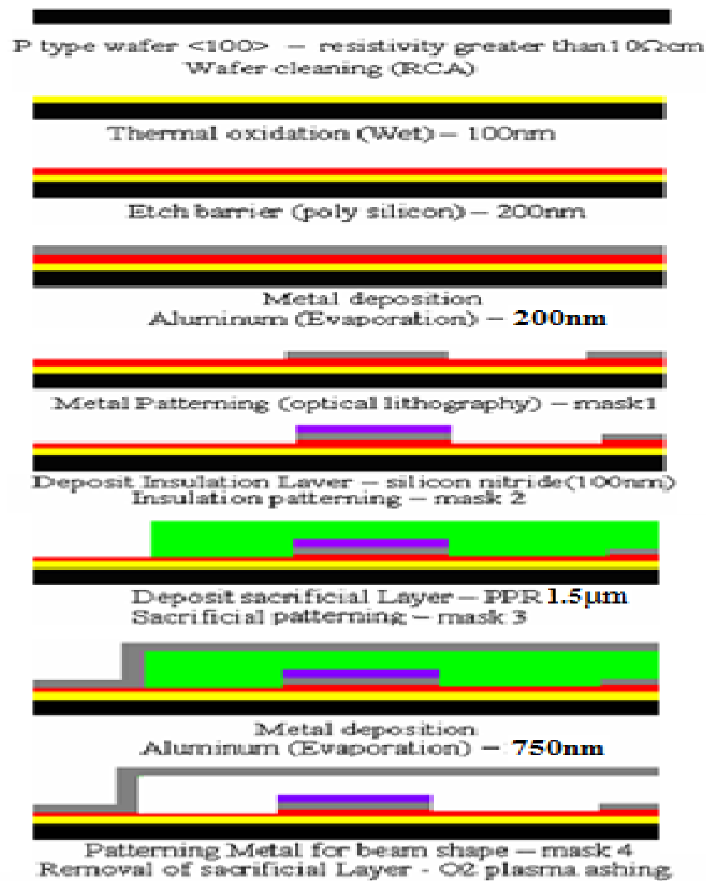


Fig 21. Fabrication Process Flow.

The mask used during lithography is prepared using AUTOCAD and then the mask is printed and stuck on a glass plate to be used during optical lithography UV exposure. It is 4-level mask fabrication processes , mask design is as shown in Fig 22.

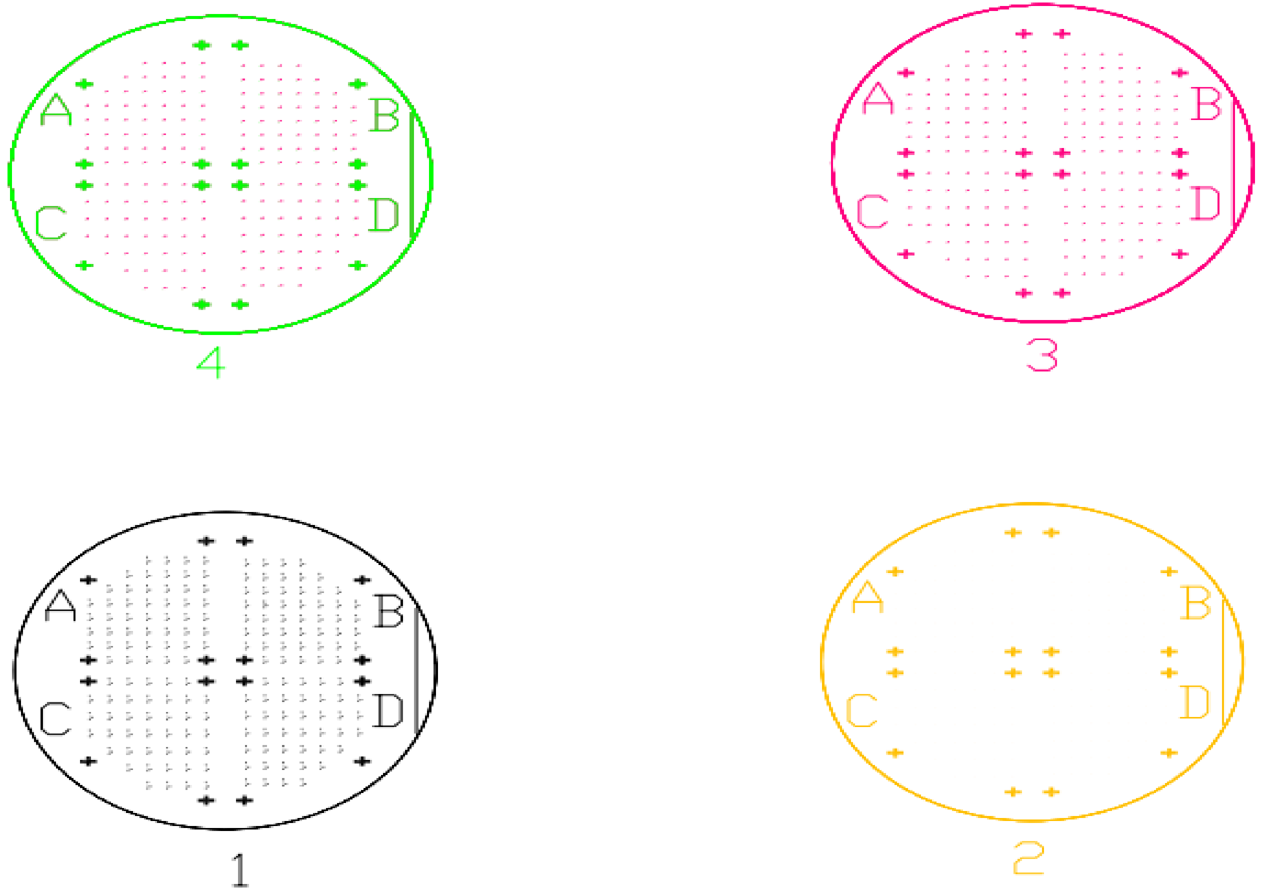


Fig. 22. Mask Design

The stepwise process details used for fabrication are as follows:

• P-type wafer (100) orientation of high resistivity which allows the possibility for integration with CMOS for multifunction assemblies say more than 10Ωcm is used.

• Wafer cleaning→ Same process discussed in section 3 is used.

• Thermal oxidation (SiO_2) – Same process discussed in section 3 is used.

• Amorphous Polysilicon Deposition [IPCVD] – Amorphous polysilicon of 200nm thickness is deposited using inductively coupled chemical vapour deposition [IPCVD]. Amorphous polysilicon is used as etch barrier.

• Metal deposition – Aluminium [0.20µm]

The aluminium used as bottom metal has been evaporated using thermal evaporator. In this

process, the metal (aluminum) is heated in vacuum so that it evaporates and gets deposited over the wafer. Maintaining the vacuum is very important here. The thickness of the metal deposited depends on the metal weight. Same process discussed in section3 is used for aluminium deposition.

• 1st level Lithography- Same process discussed in section 3 is used.

• Silicon nitride Deposition [ICPCVD]

The dielectric silicon nitride of 100nm thickness has been deposited using inductively coupled plasma chemical Vapour Deposition technique.

• 2nd level Lithography -The patterning of silicon nitride has been done using optical lithography. The selective etching of silicon nitride has been done using dry etching (RIE- Reactive ion etching).

• Deposition of PPR (positive photoresist -SU 1813) as sacrificial layer. The PPR of 1.5 μm thickness is coated using spinner at speed 3000rpm for 30 sec.

•3rd level Lithography-Patterning PPR to form anchor.

• Deposition of Metal (Aluminium)-Top metal of 750 nm thickness is deposited using thermal evaporator in order to create the cantilever beam after lithography.

•4th level Lithography -Patterning metal layer to form beam. The dehydration step should be avoided because PPR is used as sacrificial layer

• Removal of Sacrificial Layer (PPR) – O_2 plasma ashing.

A lot of optimization has been done in O_2 plasma ashing (dry etching) with respect to RF power & ashing time to get full removal of positive photoresist (PPR) .

Following images are the step taken after each fabrication process steps of MEMS cantilever switch.

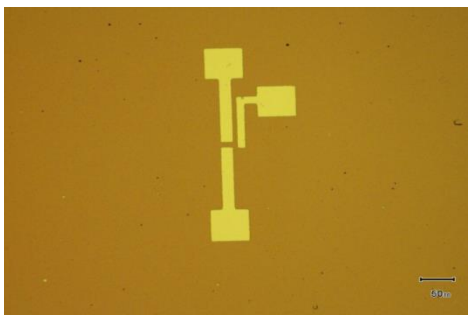


Fig. 23. Patterned bottom electrode (Al) and transmission line pads.

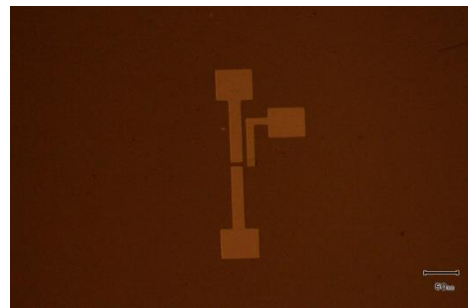


Fig. 24. Patterned dielectric (Si_3H_4).

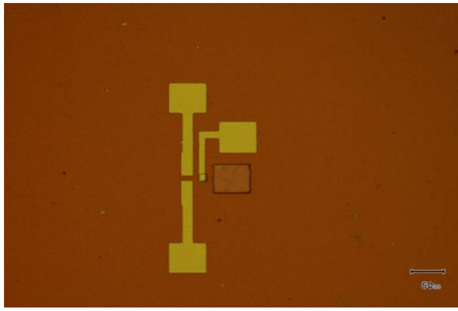


Fig. 25. Creating cavity for top electrode contact.

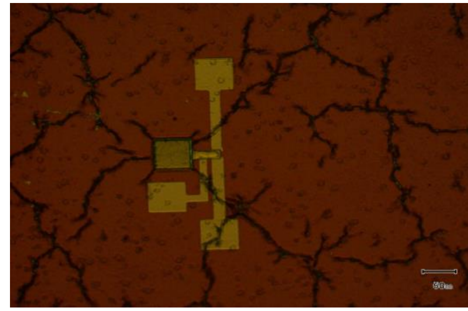


Fig. 26. Patterned beam shape.

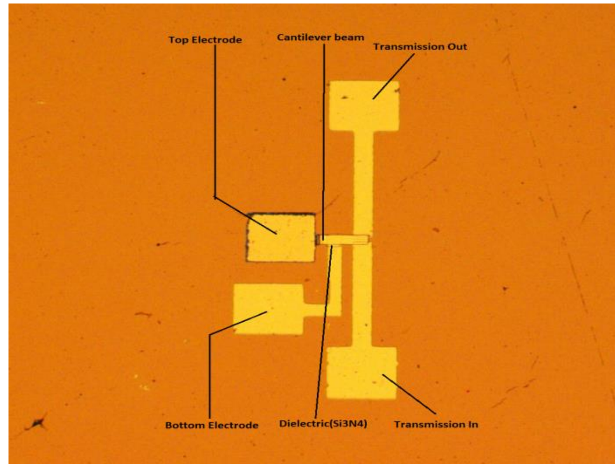


Fig.27. MEMS cantilever switch

To verified PPR is removed below the cantilever beam SEM image is taken. Top view & cross sectional view SEM images is taken by Raith -150 instrument.

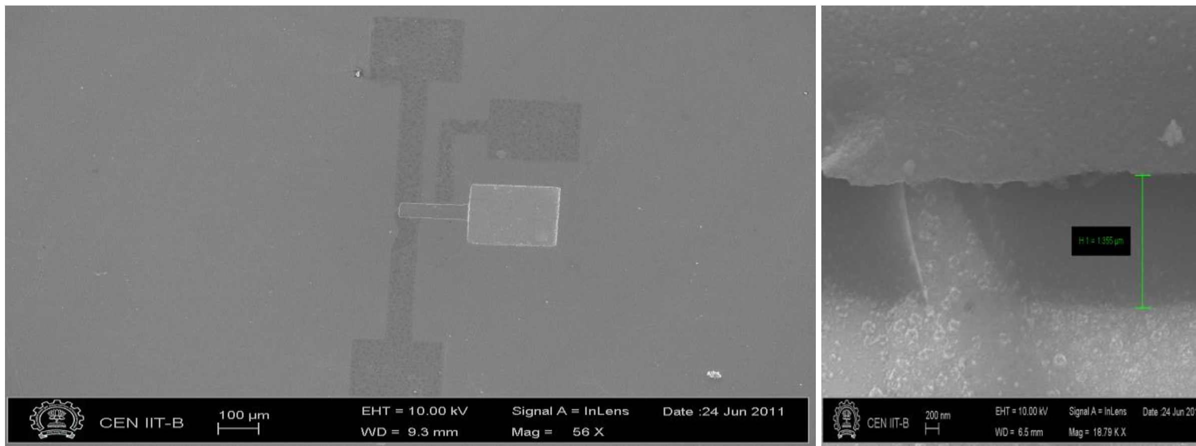


Fig. 28.Top view &Cross sectional view of MEMS switch

6. ELECTRICAL CHARACTERIZATION OF MICROCANTILEVER SWITCH

Electrical characterization is carried out to verify the functionality of the device and to study the reliability issues.Electrical characterization setup discussed in section 4 , is used for measurement.

6.1 PULL-IN AND PULL-OUT VOLTAGE

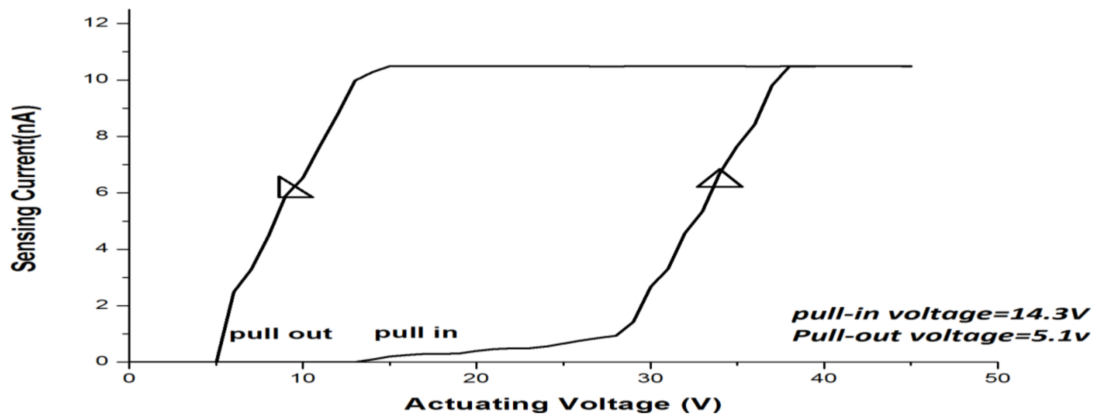


Fig. 29. Current - Voltage characteristics of MEMS cantilever switch.

The MEMS cantilever switch has been characterized by current v/s voltage characteristics to study conduction mechanism and trap properties in the silicon nitride. The applied voltage was swept from 0V to 45V between bottom electrode & top beam result in pull-in voltage at 14.3V. When sweep voltage from 45 to 0 V is applied between bottom electrode & top beam result in pull-out voltage at 5.1V.The actuation voltage of switch is coming at 38V when top beam is come in contact with bottom electrode & current remain constant. The hysteresis in voltage appears during ON-OFF cycle of electrostatic actuated MEMS switches, as shown in Fig. 29. It arises from the transition between stable and unstable equilibrium states of the switch. An electrostatic actuated switch requires a voltage higher than pull-in voltage to go ON, but it needs a voltage just higher than pull-out voltage to remain ON.

6.2 CURRENT - VOLTAGE CHARACTERIZATION

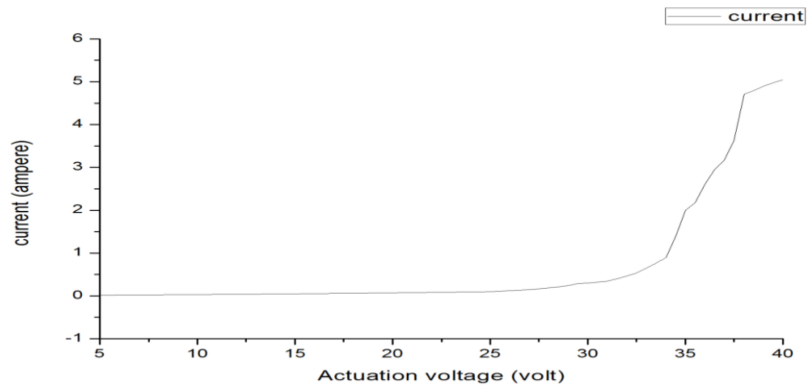


Fig. 30. Current – Voltage characterization between the transmission pad and actuation voltage

Here we applied actuating voltage from 0 to 40V between bottom electrode & top beam while maintaining a voltage bias of 10V across strips line. As per the desired functionality of switch the strip lines should form a short path and conduct current as soon as the cantilever is actuated due to applied voltage at the actuation electrode. The graph is showing the current flowing from one contact of transmission pad to another pad of transmission pad.

From fig. 29. results verifies a successful fabrication of a MEMS Cantilever switch. It shows that when applied voltage switches from zero potential to magnitude of 40v, the strip lines get short and as we can observe current flowing through the strip lines.

6.3 LIFE TIME CHARACTERIZATION OF MEMS SWITCH

In order to study the reliability of MEMS Switch ,life time characterization is performed to find out the till how much time it can work without stiction.

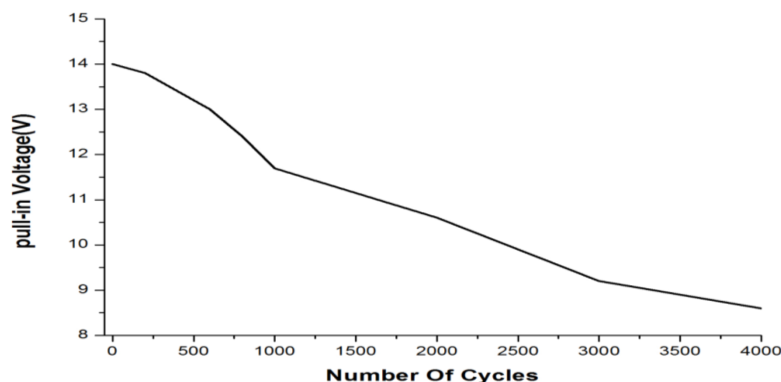


Fig. 31. Pull-in voltage v/s Number of Cycles

When continuous pulses of step input voltage 0 & 40 V is applied to top & bottom electrode i.e applying step voltage (0-40v) of pulses ranging from 0,500,1000,1500,2000 till 4000 pulse result in change in pull-in voltage of beam. When no pulses are applied result in pull-in voltage at 14.3V and after 4000 pulses is applied result in pull-in voltage at 8.6V. From Fig 23. we observed pull-in voltage is slight decreasing after every 500 pulses applied .It is due to charge trapping phenomenon in the dielectric resulting in early pull-in of MEMS switch.

6.4 CAPACIATNACE -VOLTAGE CHARACTERIZATION AFTER PULSES

The switch has been actuated many cycles during the C-V measurement to check the in use stiction. Here we applied sweep voltage and measured corresponding value of capacitance between the top and bottom electrode after every pulse. The switch responded continuously without being stuck

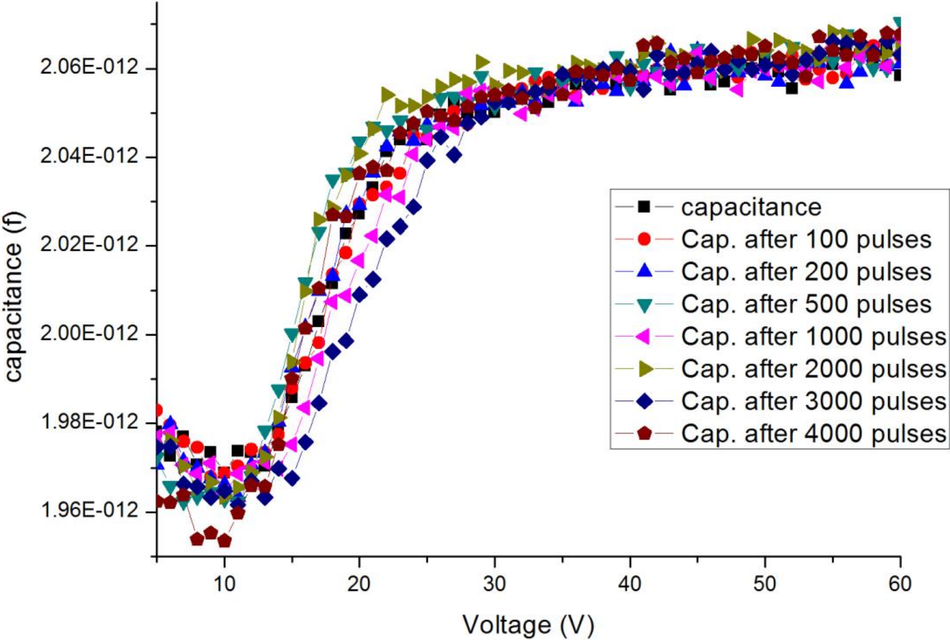


Fig. 32. Capacitance v/s Voltage after pulses.

Fig. 31. shows fresh C-V curve and C-V curve after pulses applied ex: 100, 200, 500, and 1000 till 4000 pulses. This shows that even after 4000 pulses we are getting almost same transitions in capacitance curve after every pulse. The switch responded continuously without being stuck.

7. CONCLUSION

The stiction is a major cause of failure in MEMS cantilever switches. The stiction depends on dielectric charging which is related to actuation voltage. We have Fabricated Metal-Insulator-Metal (MIM) capacitor structure with same electrode and dielectric material as that of switch deposited using HWCVD and ICPCVD Methods to study the effect of deposition condition on physical and electrical characterization of the switch. Measurements from Atomic Force Microscopy show that the ICPCVD films has more uniform surface than HWCVD films. Stabilized field in ICPCVD films enhances its performance in the electrical domain and thus effects like low leakage, high breakdown and considerable performance after stressing were observed. We have fabricated microcantilever switch by considering the background of experimental observations in Test structure. Electrical characterization is carried out to check the functionality of the device, the results of characterization verify expected functionality of switch.

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